1.5 to 18 V (4.5 to 25 V bias) Input, 12-A Synchronous Step-Down SWIFT™ Converter With PMBus™

Check for Samples: TPS53915

FEATURES

- **Integrated 13.8 and 5.9 mΩ MOSFETs Support 12-A Continuous Output Current**
- **Adjustments Available Via PMBus™**
  - **Voltage Margin and Adjustment**
  - **Soft-Start Time**
  - **Power-On Delay**
  - **VDD UVLO Level**
  - **Fault Reporting**
  - **Switching Frequency**
- **Supports All Ceramic Output Capacitors**
- **Reference Voltage 600 mV ±0.5% Tolerance**
- **Output Voltage Range: 0.6 V to 5.5 V**
- **D-CAP3™ Control Mode With Fast Load-Step Response**
- **Auto-Skipping Eco-mode™ for High Light-Load Efficiency**
- **FCCM for Tight Output Ripple and Voltage Requirements**
- **Eight Selectable Frequency Settings from 200 kHz to 1 MHz**
- **3.5 mm × 4.5 mm, 28-Pin, QFN Package**

APPLICATIONS

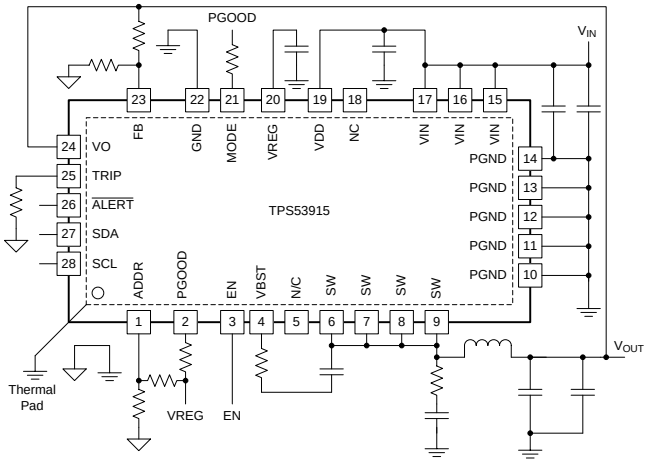
- **Server and Cloud-Computing Point-of-Load (POL) Products**
- **Broadband, Networking, and Optical Communications Infrastructure**
- **I/O Supplies**
- **Supported at the WEBENCH™ Design Center**

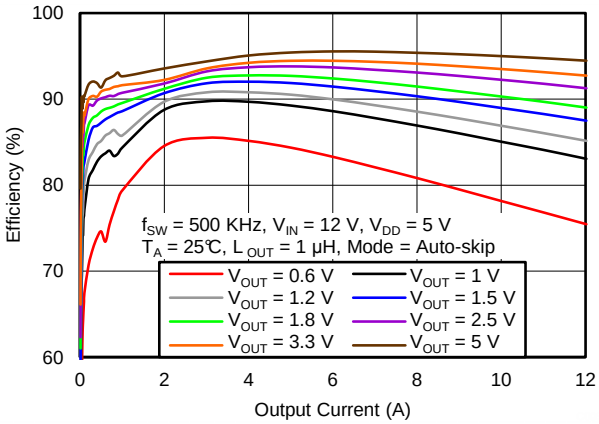
DESCRIPTION

The TPS53915 is a small-sized, synchronous buck converter with an adaptive on-time D-CAP3 control mode. The device offers ease-of-use and low external-component count for space-conscious power systems.

This device features high-performance integrated MOSFETs, accurate 0.5% 0.6-V reference, and an integrated boost switch. Competitive features include very-low external-component count, fast load-transient response, auto-skip mode operation, internal soft-start control, and no requirement for compensation. The device also features programmability and fault report via PMBus™ to simplify the power supply design.

A forced continuous conduction mode helps meet tight voltage regulation accuracy requirements for performance DSPs and FPGAs. The TPS53915 is available in a 28-pin QFN package and is specified from –40°C to 85°C ambient temperature.





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PMBus is a trademark of SMIF, Inc.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			VALUE		UNIT
			MIN	MAX	
Input voltage range(2)	EN		–0.3	7.7	V
	SW	DC	–3	30	
		Transient < 10 ns	–5	32	
	VBST		–0.3	36	
	VBST(3)		–0.3	6	
	VBST when transient < 10 ns			38	
	VDD		–0.3	28	
	VIN		–0.3	30	
	ADDR, FB, MODE, SDA, SCL, VO		–0.3	6	
Output voltage range	PGOOD		–0.3	7.7	V
	$\overline{\text{ALERT}}$, TRIP, VREG		–0.3	6	
Temperature	Junction, T_J		–40	150	°C
	Storage, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground terminal.
(3) Voltage values are with respect to the SW terminal.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS53915 RVE 28 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	37.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	34.1	
θ_{JB}	Junction-to-board thermal resistance(4)	18.1	
ψ_{JT}	Junction-to-top characterization parameter(5)	1.8	
ψ_{JB}	Junction-to-board characterization parameter(6)	18.1	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	2.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage range	EN	–0.1	7	V
	SW	–3	27	
	VBST	–0.1	28	
	VBST(1)	–0.1	5.5	
	VDD	4.5	25	
	VIN	1.5	18	
	ADDR, FB, MODE, SDA, SCL, VO	–0.1	5.5	
Output voltage range	PGOOD	–0.1	7	V
	$\overline{\text{ALERT}}$, TRIP, VREG	–0.1	5.5	
T_A	Operating free-air temperature	–40	85	°C

(1) Voltage values are with respect to the SW pin.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, V_{REG} = 5 V, V_{EN} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{VDD}	VDD bias current	T_A = 25°C, No load Power conversion enabled (no switching)		1350	1850	µA
$I_{VDDSTBY}$	VDD standby current	T_A = 25°C, No load Power conversion disabled		850	1150	µA
$I_{VIN(leak)}$	VIN leakage current	V_{EN} = 0 V			0.5	µA
VREF OUTPUT						
V_{VREF}	Reference voltage	FB w/r/t GND, T_A = 25°C	597	600	603	mV
$V_{VREFTOL}$	Reference voltage tolerance	FB w/r/t GND, T_J = 0°C to 85°C	–0.6%		0.5%	
		FB w/r/t GND, T_J = –40°C to 85°C	–0.7%		0.5%	
OUTPUT VOLTAGE						
I_{FB}	FB input current	V_{FB} = 600 mV		50	100	nA
I_{VODIS}	VO discharge current	V_{VO} = 0.5 V, Power Conversion Disabled	10	12	15	mA
INTERNAL DAC REFERENCE						
$V_{DACTOL1}$	DAC voltage tolerance 1	FB w/r/t GND, 0°C ≤ T_A ≤ 85°C, with certain VOUT_ADJUSTMENT settings only (1)	–4.8		4.8	mV
$V_{DACTOL2}$	DAC voltage tolerance 2	FB w/r/t GND, 0°C ≤ T_A ≤ 85°C, with certain VOUT_MARGIN settings only (2)	–4.8		4.8	mV
$V_{DACTOL3}$	DAC voltage tolerance 3	FB w/r/t GND, 0°C ≤ T_A ≤ 85°C, with VOUT_ADJUSTMENT=0Dh and VOUT_MARGIN=70h for 5%	–4.8		4.8	mV
$V_{DACTOL4}$	DAC voltage tolerance 4	FB w/r/t GND, 0°C ≤ T_A ≤ 85°C, with VOUT_ADJUSTMENT=13h and VOUT_MARGIN=07h for -5%	–4.8		4.8	mV
SMPS FREQUENCY						
f_{SW}	VO switching frequency	V_{IN} = 12 V, V_{VO} = 3.3 V, FS<2:0> = 000		250		kHz
		V_{IN} = 12 V, V_{VO} = 3.3 V, FS<2:0> = 001		300		
		V_{IN} = 12 V, V_{VO} = 3.3 V, FS<2:0> = 010		400		
		V_{IN} = 12 V, V_{VO} = 3.3 V, FS<2:0> = 011		500		
		V_{IN} = 12 V, V_{VO} = 3.3 V, FS<2:0> = 100		600		
		V_{IN} = 12 V, V_{VO} = 3.3 V, FS<2:0> = 101		750		
		V_{IN} = 12 V, V_{VO} = 3.3 V, FS<2:0> = 110		850		
		V_{IN} = 12 V, V_{VO} = 3.3 V, FS<2:0> = 111		1000		
$t_{ON(min)}$	Minimum on-time	T_A = 25°C (3)		60		ns
$t_{OFF(min)}$	Minimum off-time	T_A = 25°C	175	240	310	ns
INTERNAL BOOTSTRAP SW						
V_F	Forward Voltage	$V_{VREG–VBST}$, T_A = 25°C, I_F = 10 mA		0.15	0.25	V
I_{VBST}	VBST leakage current	T_A = 25°C, V_{VBST} = 33 V, V_{SW} = 28 V		0.01	1.5	µA
LOGIC THRESHOLD						
V_{ENH}	EN enable threshold voltage		1.3	1.4	1.5	V
V_{ENL}	EN disable threshold voltage		1.1	1.2	1.3	V
V_{ENHYST}	EN hysteresis voltage			0.22		V
V_{ENLEAK}	EN input leakage current		–1	0	1	µA

(1) Tested at these VOUT_ADJUSTMENT settings: -9.0%, -8.25%, -5.25%, -2.25%, 0.0%, 3.00%, 6.00%, 9.0%
(2) Tested at these VOUT_MARGIN settings: -11.62%, -10.74%, -7.06%, -3.15%, 0%, 3.7%, 7.74%, 12.05%
(3) Specified by design. Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range, V_{REG} = 5 V, V_{EN} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SOFT-START						
t_{SS}	Soft-start time	SST <1:0> = 00		1		ms
		SST <1:0> = 01		2		
		SST <1:0> = 10		4		
		SST <1:0> = 11		8		
POWER GOOD COMPARATOR						
V_{PGTH}	PGOOD threshold	PGOOD in from higher	104%	108%	111%	
		PGOOD in from lower	89%	92%	96%	
		PGOOD out to higher	113%	116%	120%	
		PGOOD out to lower	80%	84%	87%	
t_{PGDLY}	PGOOD delay time	Delay for PGOOD going in PGD<2:0>=000	165	256	320	µs
		Delay for PGOOD going in PGD<2:0>=001	409	512	614	µs
		Delay for PGOOD going in PGD<2:0>=010	0.819	1.024	1.228	ms
		Delay for PGOOD going in PGD<2:0>=011	1.638	2.048	2.458	ms
		Delay for PGOOD going in PGD<2:0>=100	3.276	4.096	4.915	ms
		Delay for PGOOD going in PGD<2:0>=101	6.553	8.192	9.83	ms
		Delay for PGOOD going in PGD<2:0>=110	13.104	16.38	19.656	ms
		Delay for PGOOD going in PGD<2:0>=111	105	131	157	ms
		Delay tolerance for PGOOD coming out		2		µs
I_{PG}	PGOOD sink current	V_{PGOOD} = 0.5 V	4	6		mA
I_{PGLK}	PGOOD leakage current	V_{PGOOD} = 5.0 V	–1	0	1	µA
POWER-ON DELAY						
t_{PODLY}	Power-on delay time	Delay from enable to switching POD<2:0>=000		356		µs
		Delay from enable to switching POD<2:0>=001		612		µs
		Delay from enable to switching POD<2:0>=010		1.124		ms
		Delay from enable to switching POD<2:0>=011		2.148		ms
		Delay from enable to switching POD<2:0>=100		4.196		ms
		Delay from enable to switching POD<2:0>=101		8.292		ms
		Delay from enable to switching POD<2:0>=110		16.48		ms
		Delay from enable to switching POD<2:0>=111		32.86		ms

ELECTRICAL CHARACTERISTICS (continued)

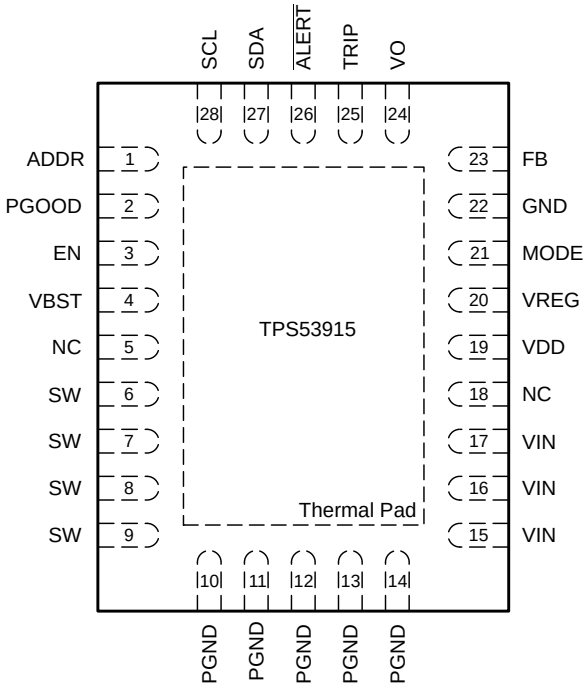
over operating free-air temperature range, V_{REG} = 5 V, V_{EN} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT DETECTION						
R_{TRIP}	TRIP pin resistance range		20		70	kΩ
I_{OCL}	Current limit threshold, valley	R_{TRIP} = 52.3 kΩ	10.1	12.0	13.9	A
		R_{TRIP} = 38 kΩ	7.2	9.1	11.0	
I_{OCLN}	Negative current limit threshold, valley	R_{TRIP} = 52.3 kΩ	–15.3	–11.9	–8.5	A
		R_{TRIP} = 38 kΩ	–12	–9	–6	
V_{ZC}	Zero cross detection offset			0		mV
PROTECTIONS						
$V_{VREGUVLO}$	VREG undervoltage-lockout (UVLO) threshold voltage	Wake-up	3.25	3.34	3.41	V
		Shutdown	3.00	3.12	3.19	
$V_{VDDUVLO}$	VDD UVLO threshold voltage	Wake-up (default)	4.15	4.25	4.35	V
		Shutdown	3.95	4.05	4.15	
V_{OVP}	Overvoltage-protection (OVP) threshold voltage	OVP detect voltage	116%	120%	124%	
t_{OVPDLY}	OVP propagation delay	With 100-mV overdrive		300		ns
V_{UVP}	Undervoltage-protection (UVP) threshold voltage	UVP detect voltage	64%	68%	71%	
t_{UVPDLY}	UVP delay	UVP filter delay		1		ms
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold(4)	Shutdown temperature		140		°C
		Hysteresis		40		
LDO VOLTAGE						
V_{REG}	LDO output voltage	V_{IN} = 12 V, I_{LOAD} = 10 mA	4.65	5	5.45	V
V_{DOVREG}	LDO low droop drop-out voltage	V_{IN} = 4.5 V, I_{LOAD} = 30 mA, T_A = 25°C			365	mV
I_{LDOMAX}	LDO over-current limit	V_{IN} = 12 V, T_A = 25°C	170	200		mA
INTERNAL MOSFETS						
$R_{DS(on)H}$	High-side MOSFET on-resistance	T_A = 25°C		13.8	15.5	mΩ
$R_{DS(on)L}$	Low-side MOSFET on-resistance	T_A = 25°C		5.9	7.0	mΩ
PMBus SCL and SDA INPUT BUFFER LOGIC THRESHOLDS						
$V_{IL-PMBUS}$	SCL and SDA low-level input voltage(4)	0°C ≤ T_J ≤ 85°C			0.8	V
$V_{IH-PMBUS}$	SCL and SDA high-level input voltage(4)	0°C ≤ T_J ≤ 85°C	2.1			V
$V_{HY-PMBUS}$	SCL and SDA hysteresis voltage(4)	0°C ≤ T_J ≤ 85°C		240		mV
PMBus SDA and $\overline{\text{ALERT}}$ OUTPUT PULLDOWN						
$V_{OL1-PMBUS}$	SDA and $\overline{\text{ALERT}}$ low-level output voltage(4)	$V_{DDPMBus}$ = 5.5 V, R_{PULLUP} = 1.1 kΩ, 0°C ≤ T_J ≤ 85°C			0.4	V
$V_{OL2-PMBUS}$	SDA and $\overline{\text{ALERT}}$ low-level output voltage(4)	$V_{DDPMBus}$ = 3.6 V, R_{PULLUP} = 0.7 kΩ, 0°C ≤ T_J ≤ 85°C			0.4	V

(4) Specified by design. Not production tested.

DEVICE INFORMATION

QFN
28-PIN
(TOP VIEW)



PIN DESCRIPTIONS(1)

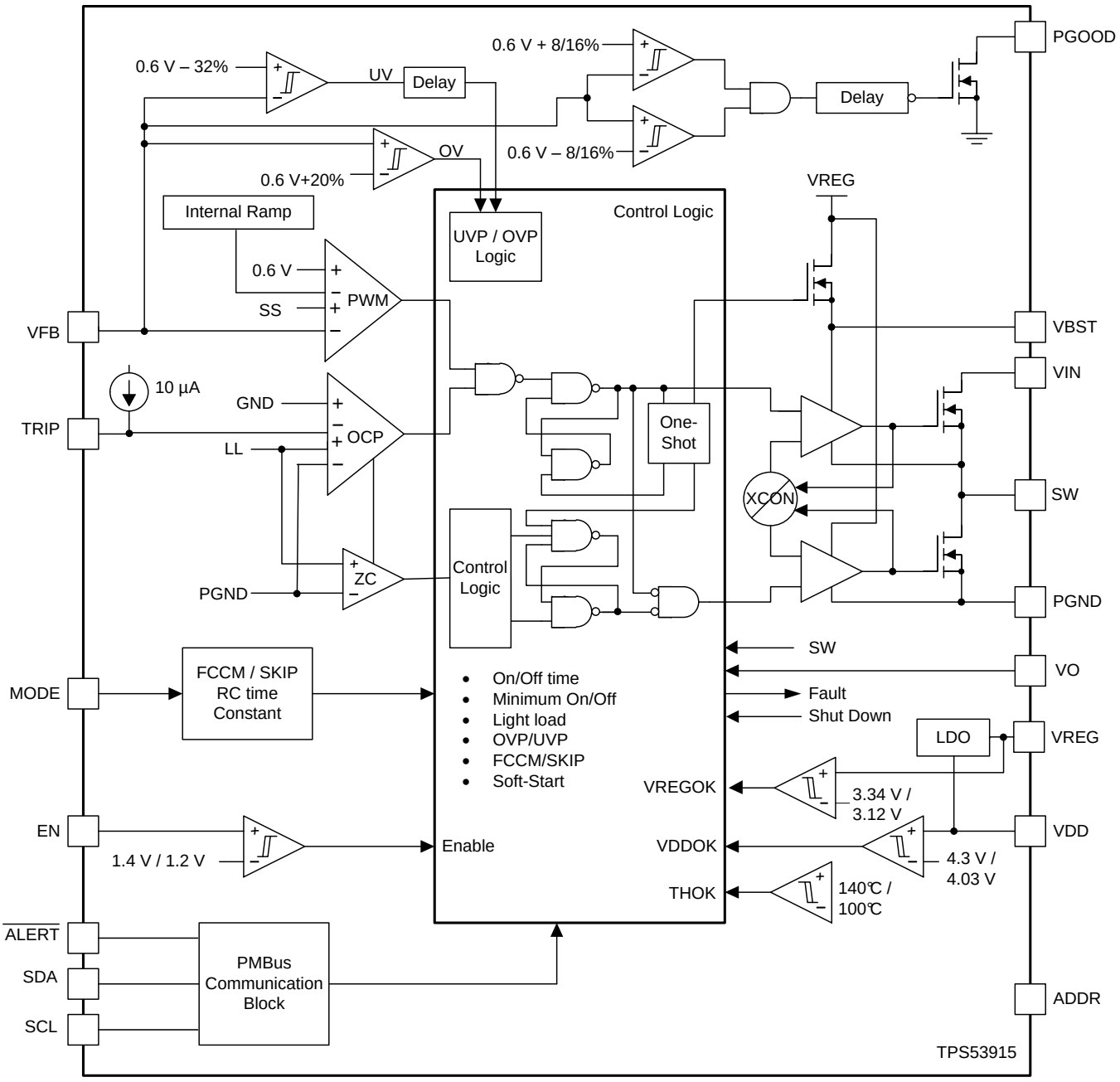
PIN		I/O	DESCRIPTION
NAME	NO.		
ADDR	1	I	PMBus address configuration pin. Connect this pin into a resistor divider between VREG and GND to program different address settings
$\overline{\text{ALERT}}$	26	O	Alert output for the PMBus interface
EN	3	I	The enable pin turns on the DC-DC switching converter.
FB	23	I	V_{OUT} feedback input. Connect this pin to a resistor divider between the VOUT pin and GND.
GND	22	G	This pin is the ground of internal analog circuitry and driver circuitry. Connect GND to the PGND plane with a short trace (For example, connect this pin to the thermal pad with a single trace and connect the thermal pad to PGND pins and PGND plane).
MODE	21	I	The MODE pin sets the forced continuous-conduction mode (FCCM) or Skip-mode operation. It also selects the ramp coefficient of D-CAP3 mode.
NC	5	—	Not connected. These pins are floating internally.
	18		
PGND	10	G	These ground pins are connected to the return of the internal low-side MOSFET.
	11		
	12		
	13		
	14		
PGOOD	2	O	Open-drain power-good status signal which provides startup delay after the FB voltage falls within the specified limits. After the FB voltage moves outside the specified limits, PGOOD goes low within 2 µs.
SCL	28	I	Clock input for the PMBus interface
SDA	27	I/O	Data I/O for the PMBus interface

(1) I = Input, O = Output, P = Supply, G = Ground

PIN DESCRIPTIONS(1) (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
SW	6	I/O	SW is the output switching terminal of the power converter. Connect this pin to the output inductor.
	7		
	8		
	9		
TRIP	25	I/O	TRIP is the OCL detection threshold setting pin. I_{TRIP} = 10 µA at T_A = 25°C, 3000 ppm/°C current is sourced and sets the OCL trip voltage. See the Current Sense and Overcurrent Protection section for detailed OCP setting.
VBST	4	P	VBST is the supply rail for the high-side gate driver (boost terminal). Connect the bootstrap capacitor from this pin to the SW node. Internally connected to VREG via bootstrap PMOS switch.
VDD	19	P	Power-supply input pin for controller. Input of the VREG LDO. The input range is from 4.5 to 25 V.
VIN	15	P	VIN is the conversion power-supply input pins.
	16		
	17		
VREG	20	O	VREG is the 5-V LDO output. This voltage supplies the internal circuitry and gate driver.
VO	24	I	VOUT voltage input to the controller.

BLOCK DIAGRAM



APPLICATION CIRCUIT DIAGRAM

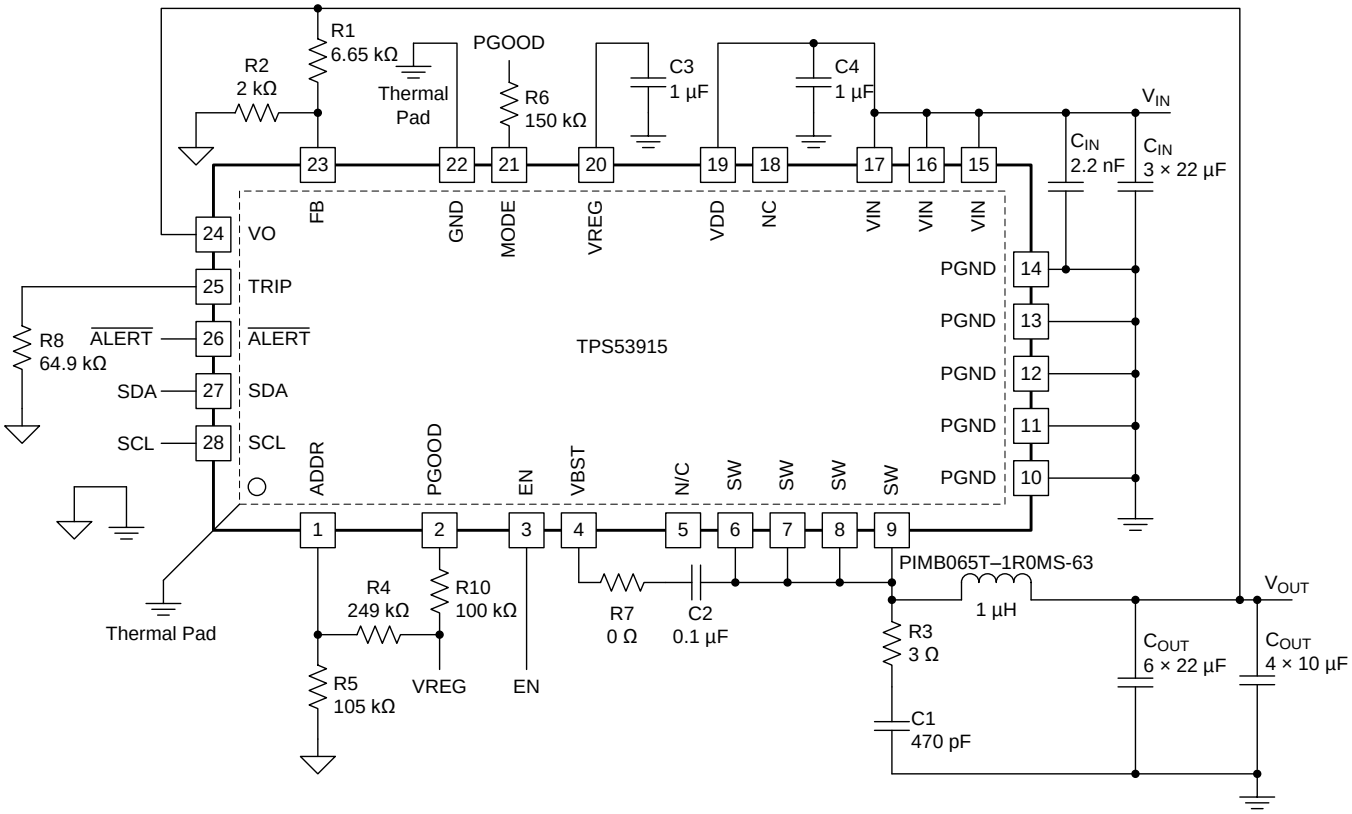


Figure 1. Typical Application Circuit Diagram

TYPICAL CHARACTERISTICS

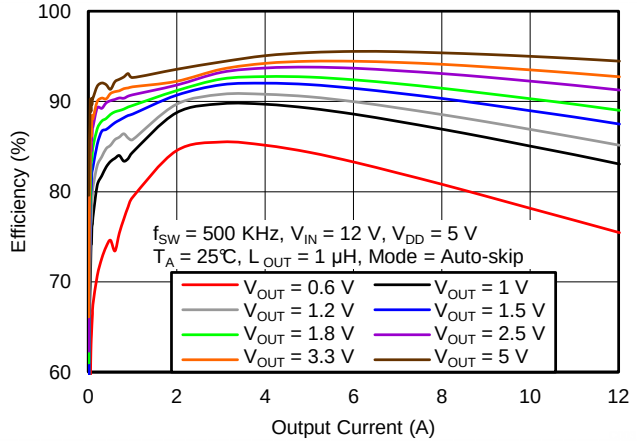


Figure 2. Efficiency vs. Output Current

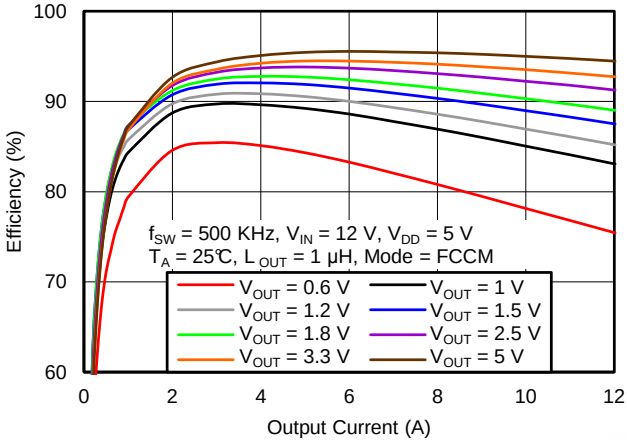


Figure 3. Efficiency vs. Output Current

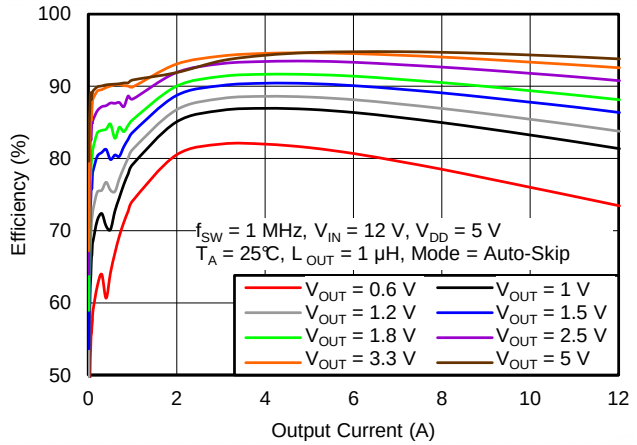


Figure 4. Efficiency vs. Output Current

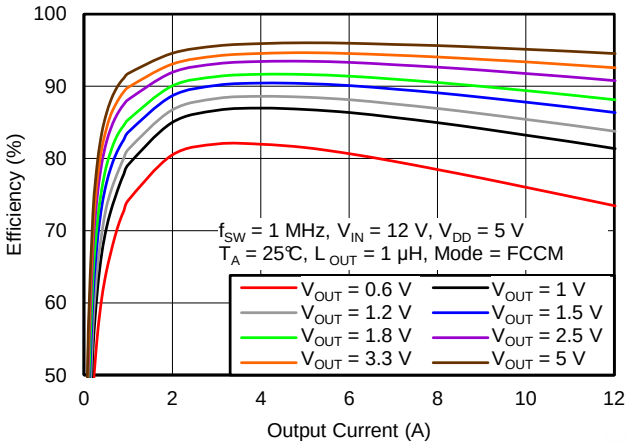


Figure 5. Efficiency vs. Output Current

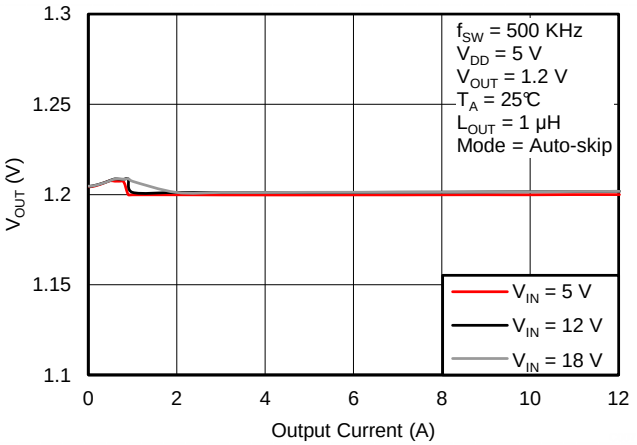


Figure 6. Output Voltage vs. Output Current

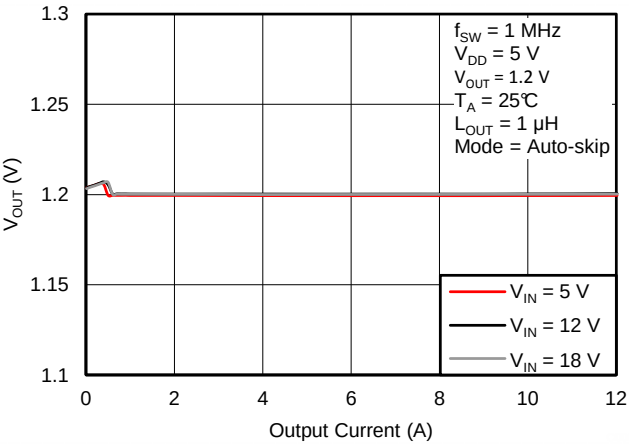


Figure 7. Output Voltage vs. Output Current

TYPICAL CHARACTERISTICS (continued)

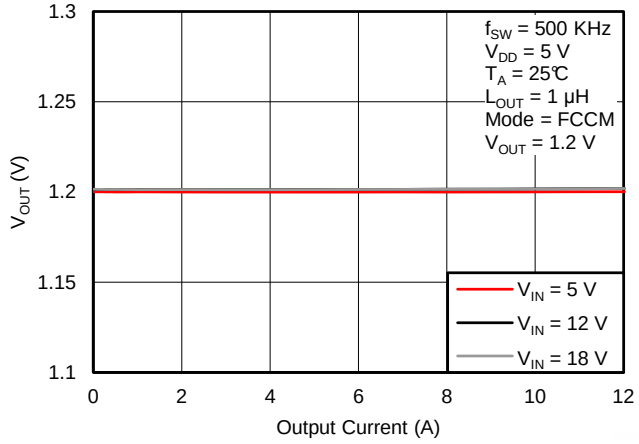


Figure 8. Output Voltage vs. Output Current

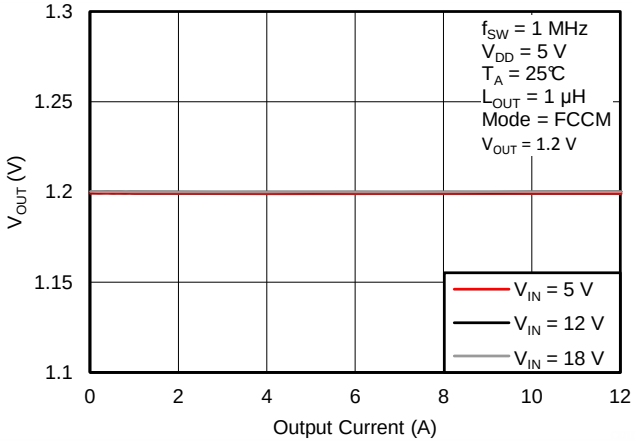


Figure 9. Output Voltage vs. Output Current

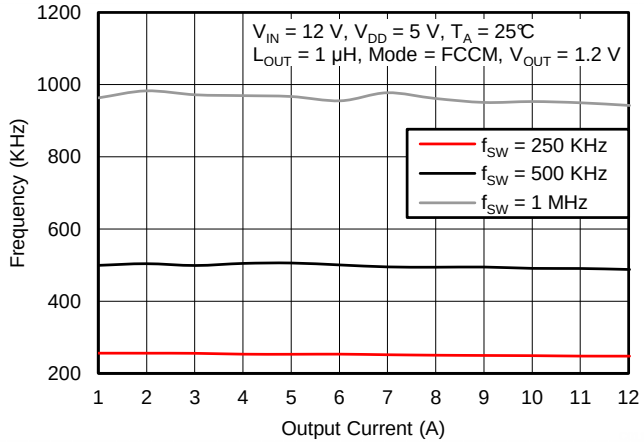


Figure 10. Switching Frequency vs. Output Current

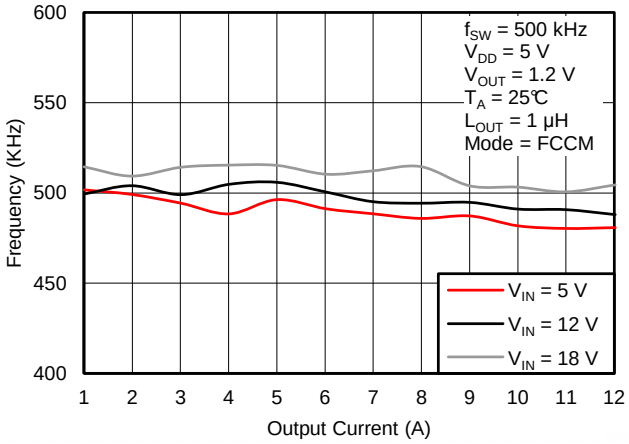


Figure 11. Switching Frequency vs. Output Current

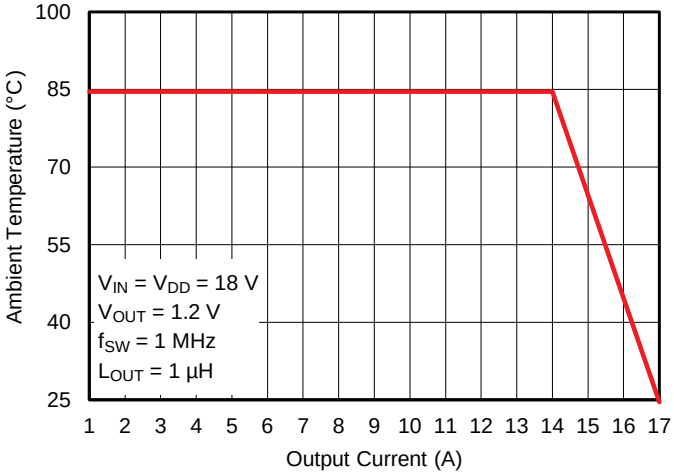


Figure 12. Safe Operating Area, V_{OUT} = 1.2 V

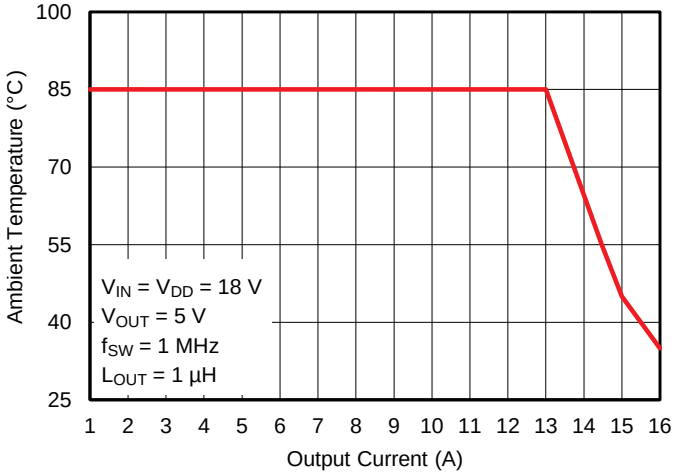


Figure 13. Safe Operating Area, V_{OUT} = 5 V

TYPICAL CHARACTERISTICS (continued)

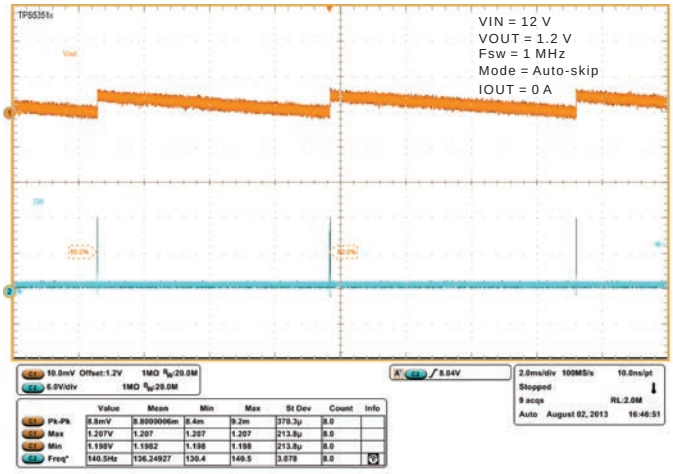


Figure 14. Auto-Skip Steady-State Operation

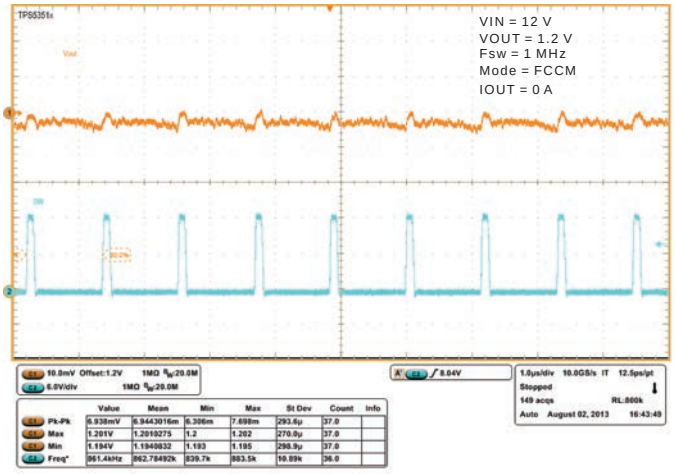


Figure 15. FCCM Steady-State Operation

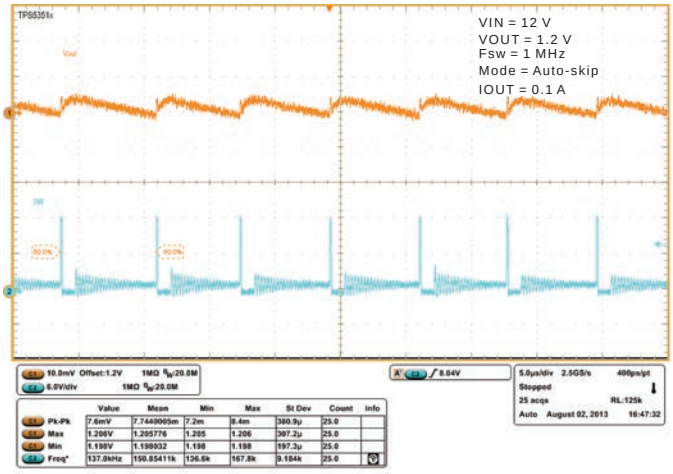


Figure 16. Auto-Skip Steady-State Operation

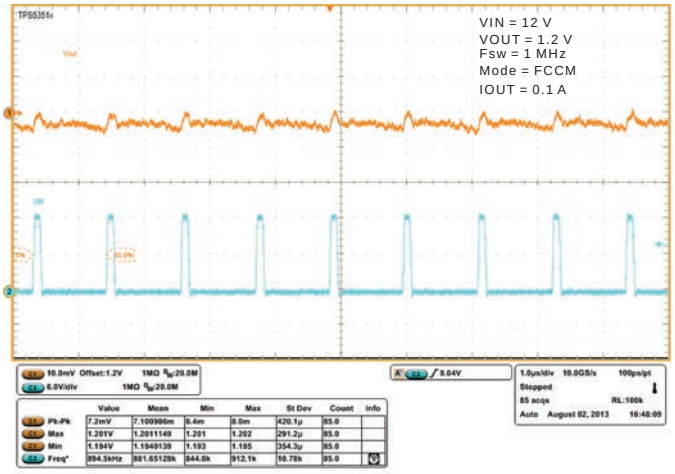


Figure 17. FCCM Steady-State Operation

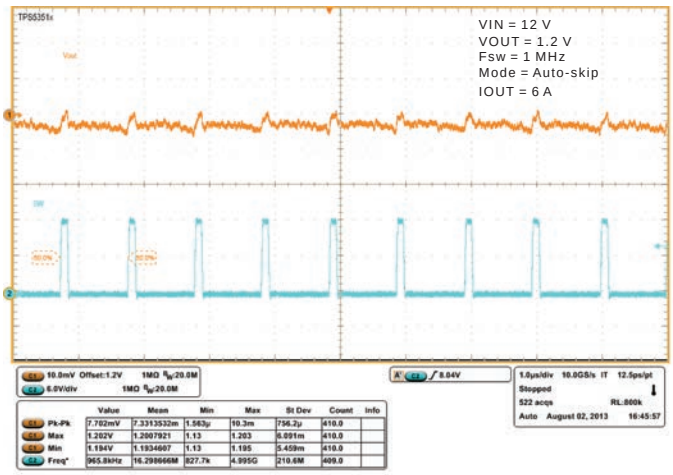


Figure 18. Auto-Skip Steady-State Operation

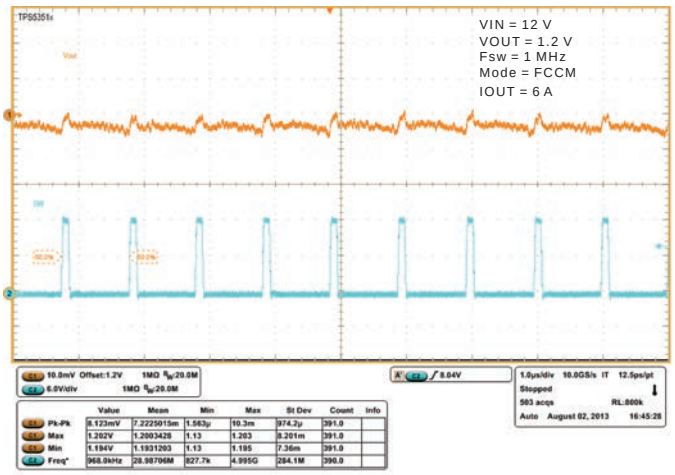


Figure 19. FCCM Steady-State Operation

TYPICAL CHARACTERISTICS (continued)

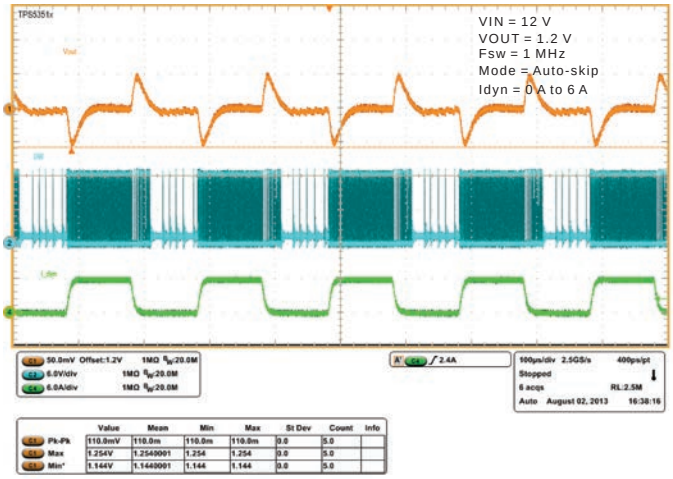


Figure 20. Auto-Skip Mode Load Transient

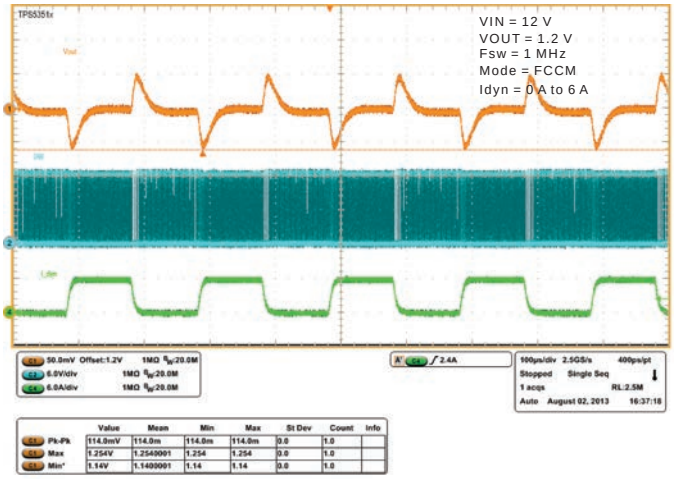


Figure 21.

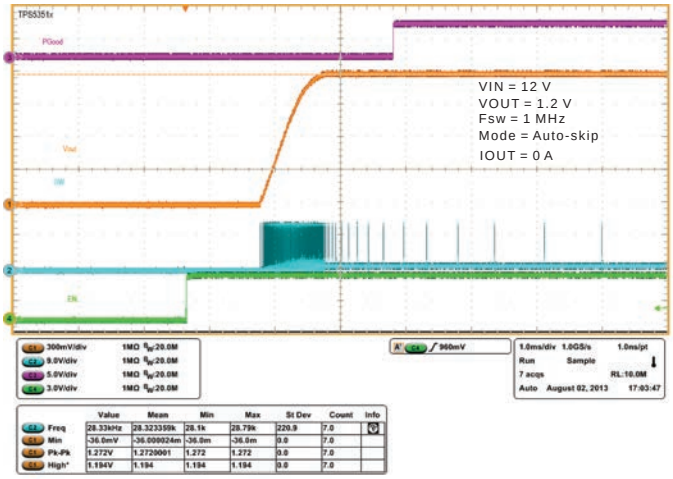


Figure 22. Start-Up

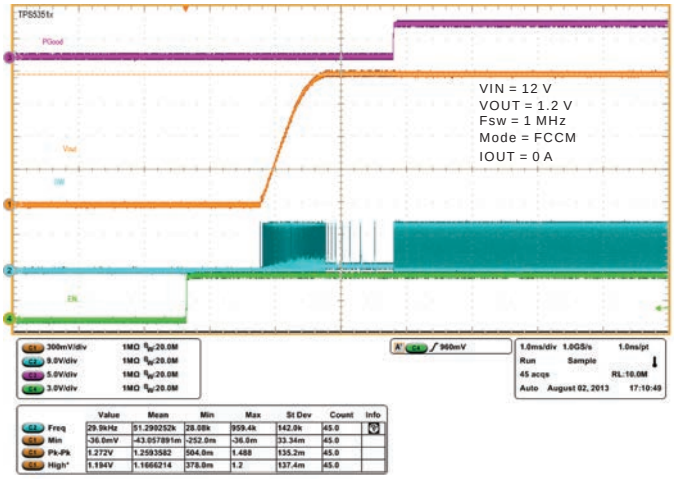


Figure 23. Start-Up

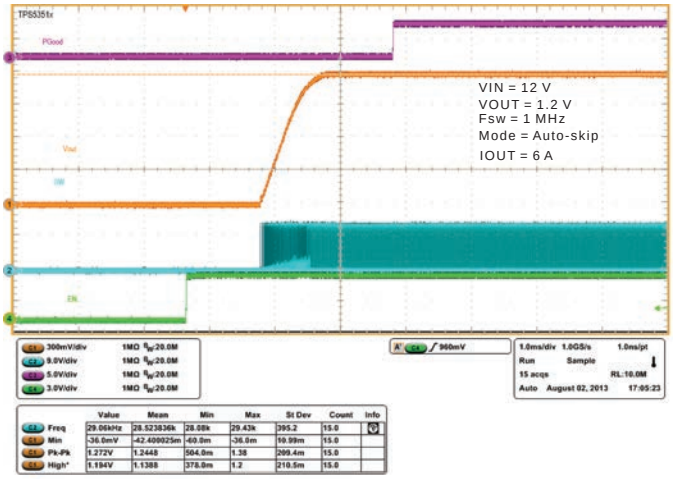


Figure 24. Start-Up

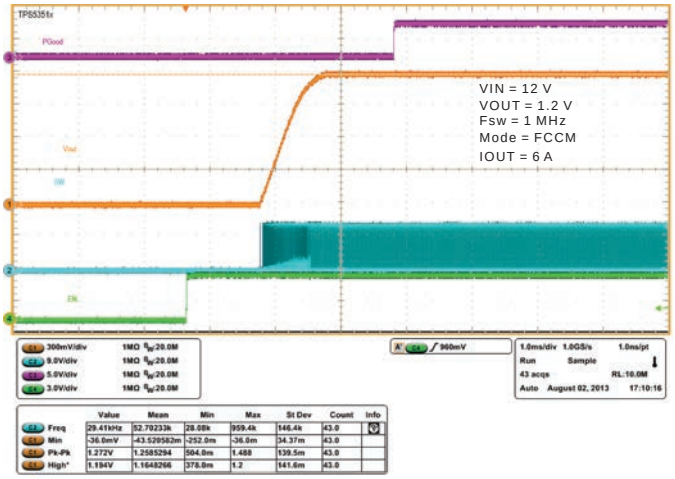


Figure 25. Start-Up

TYPICAL CHARACTERISTICS (continued)

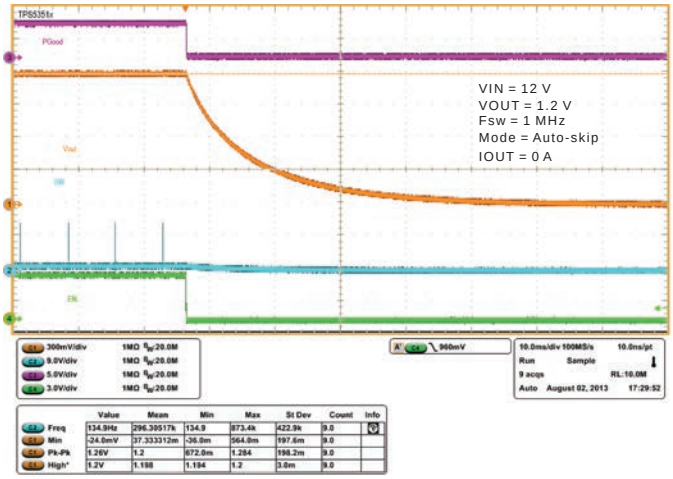


Figure 26. Shut-Down Operation

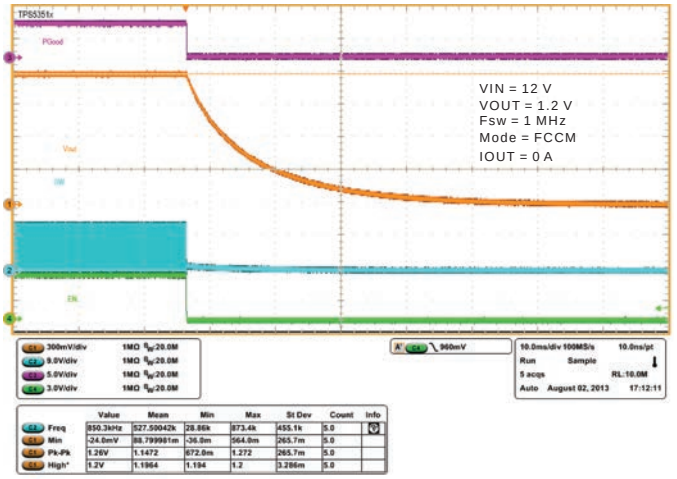


Figure 27. Shut-Down Operation

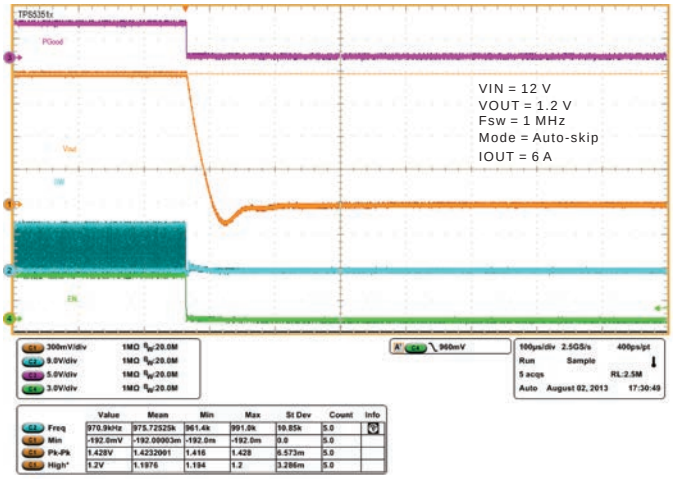


Figure 28. Shut-Down Operation

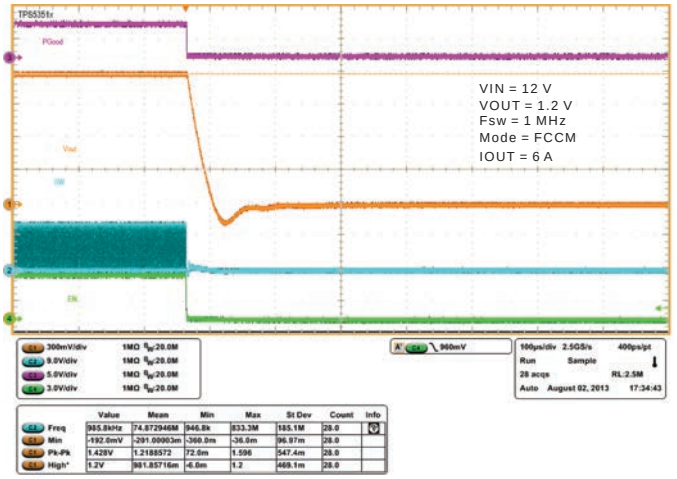


Figure 29. Shut-Down Operation

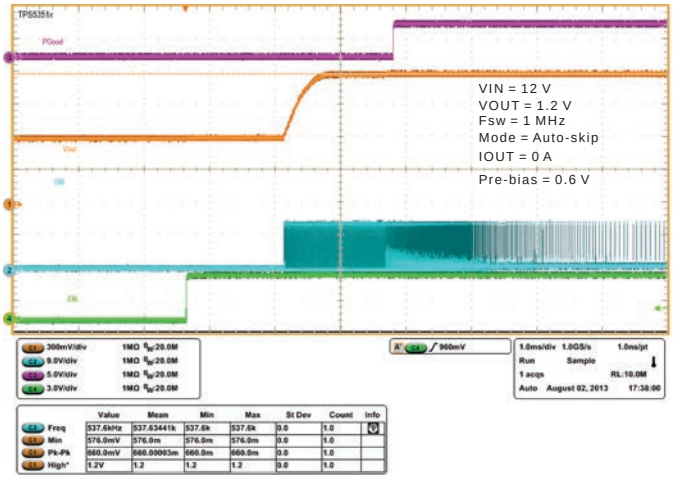


Figure 30. Pre-Bias Operation

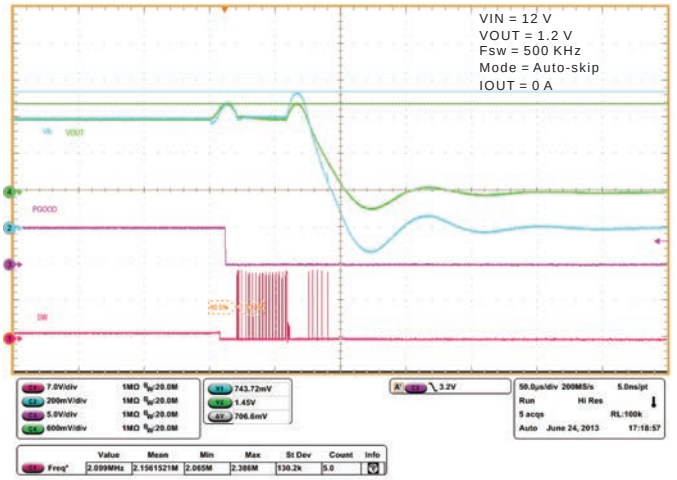


Figure 31. Overvoltage Protection

TYPICAL CHARACTERISTICS (continued)

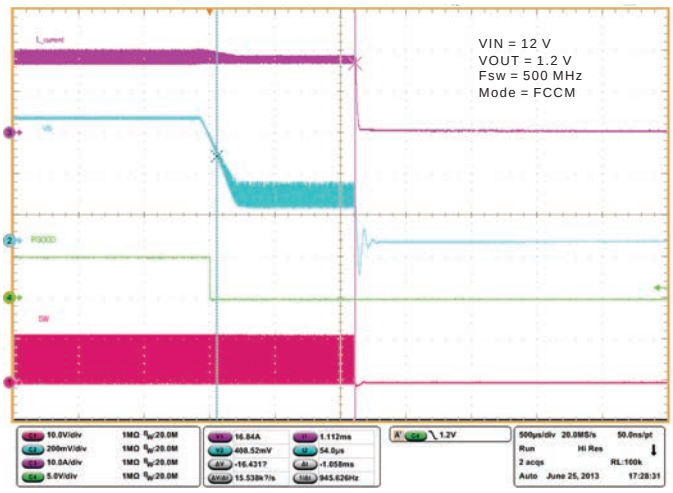


Figure 32. Overcurrent Protection

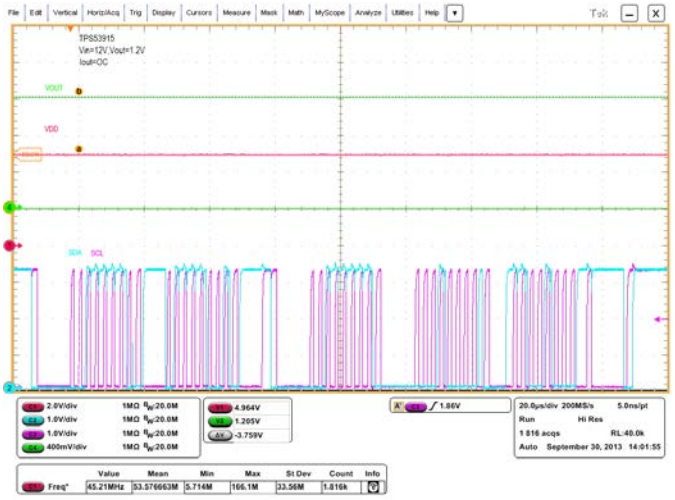


Figure 33. I^2C READ (Address=31d, Cmd=0x79): ACK 0x10C8. I_{OC} = 15 A

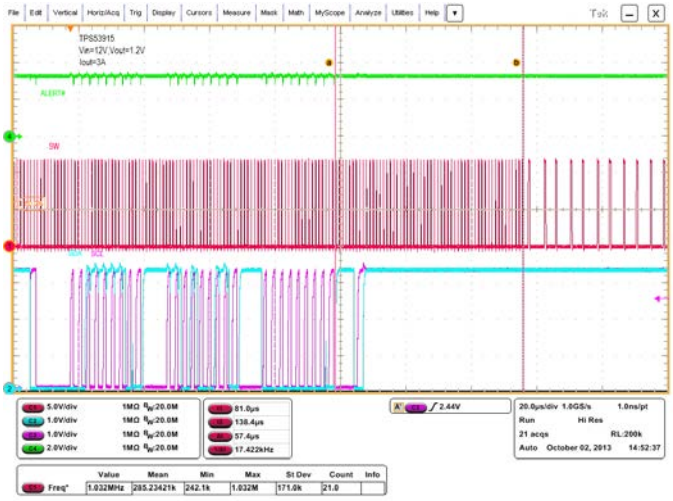


Figure 34. 1 MHz to 250 KHz

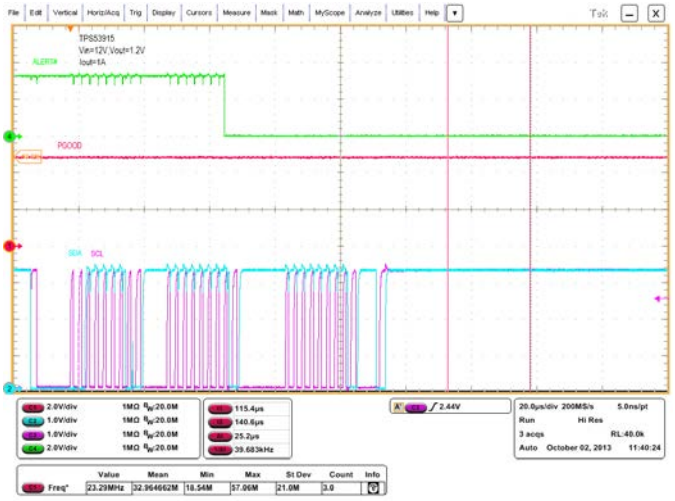


Figure 35. 31d_FFh_FFh

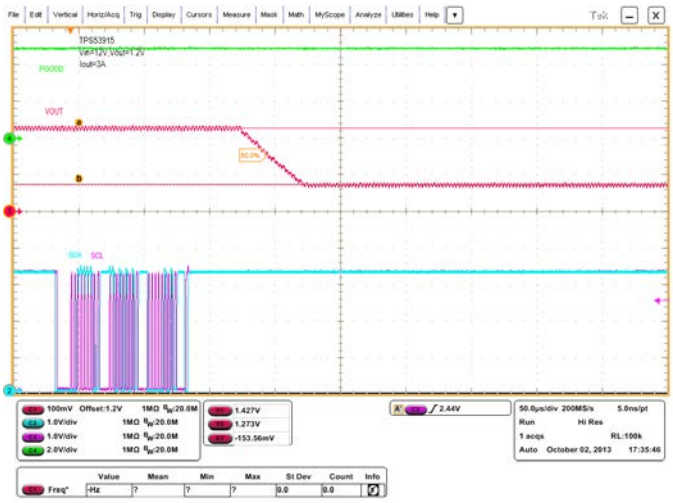


Figure 36. $V_{OUT(adj)}$ = 6%, V_{OMH} = 12% to 0%

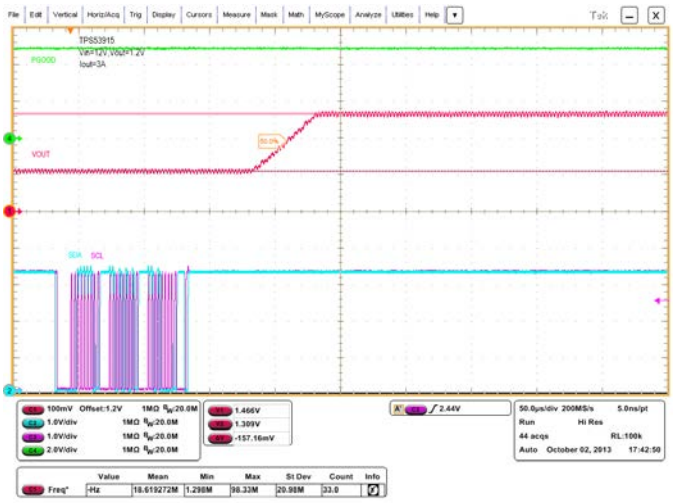


Figure 37. $V_{OUT(adj)}$ = 9%, V_{OMH} = 0% to 12%

TYPICAL CHARACTERISTICS (continued)

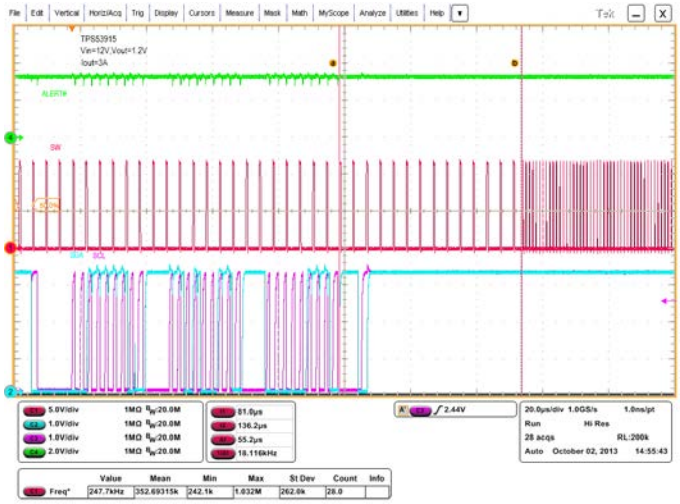


Figure 38. 250 kHz to MHz

THERMAL PERFORMANCE

f_{SW} = 500 kHz, V_{IN} = 12 V, V_{OUT} = 5 V, I_{OUT} = 12 A, C_{OUT} = 10 × 22 µF (1206, 6.3V, X5R), R_{BOOT} = 0 Ω, SNB = 3 Ω + 470 pF
Inductor: L_{OUT} = 1 µH, PCMC135T-1R0MF, 12.6 mm × 13.8 mm × 5 mm, 2.1 mΩ (typ)

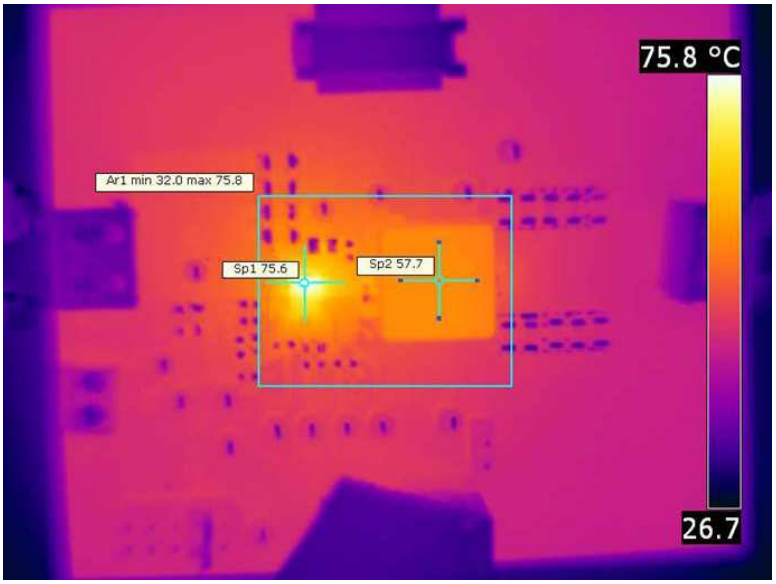


Figure 39. SP1: 75.6℃ (TPS53915), SP2: 57.7℃ (Inductor)

APPLICATION INFORMATION

General Description

The TPS53915 is a high-efficiency, single-channel, synchronous-buck converter. The device suits low-output voltage point-of-load applications with 12-A or lower output current in computing and similar digital consumer applications. The TPS53915 features proprietary D-CAP3 mode control combined with adaptive on-time architecture. This combination builds modern low-duty-ratio and ultra-fast load-step-response DC-DC converters in an ideal fashion. The output voltage ranges from 0.6 V to 5.5 V. The conversion input voltage ranges from 1.5 V to 18 V and the VDD input voltage ranges from 4.5 V to 25 V. The D-CAP3 mode uses emulated current information to control the modulation. An advantage of this control scheme is that it does not require a phase-compensation network outside which makes the device easy-to-use and also allows low-external component count. Adaptive on-time control tracks the preset switching frequency over a wide range of input and output voltage while increasing switching frequency as needed during load-step transient.

D-CAP3 Control and Mode Selection

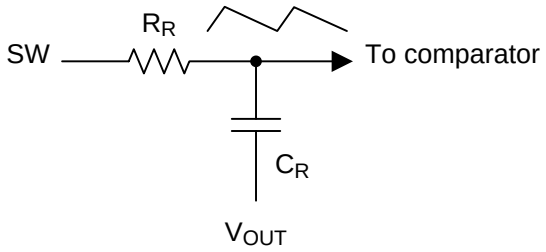


Figure 40. Internal RAMP Generation Circuit

The TPS53915 uses D-CAP3 mode control to achieve fast load transient while maintaining the ease-of-use feature. An internal RAMP is generated and fed to the VFB pin to reduce jitter and maintain stability. The amplitude of the ramp is determined by the R-C time-constant as shown in Figure 40. At different switching frequencies, (f_{SW}) the R-C time-constant varies to maintain relatively constant RAMP amplitude.

The default switching frequency (f_{SW}) is pre-set at 400 kHz. The switching frequency can be changed via PMBus function (see Table 13)

D-CAP3 Mode

From small-signal loop analysis, a buck converter using the D-CAP3 mode control architecture can be simplified as shown in Figure 41.

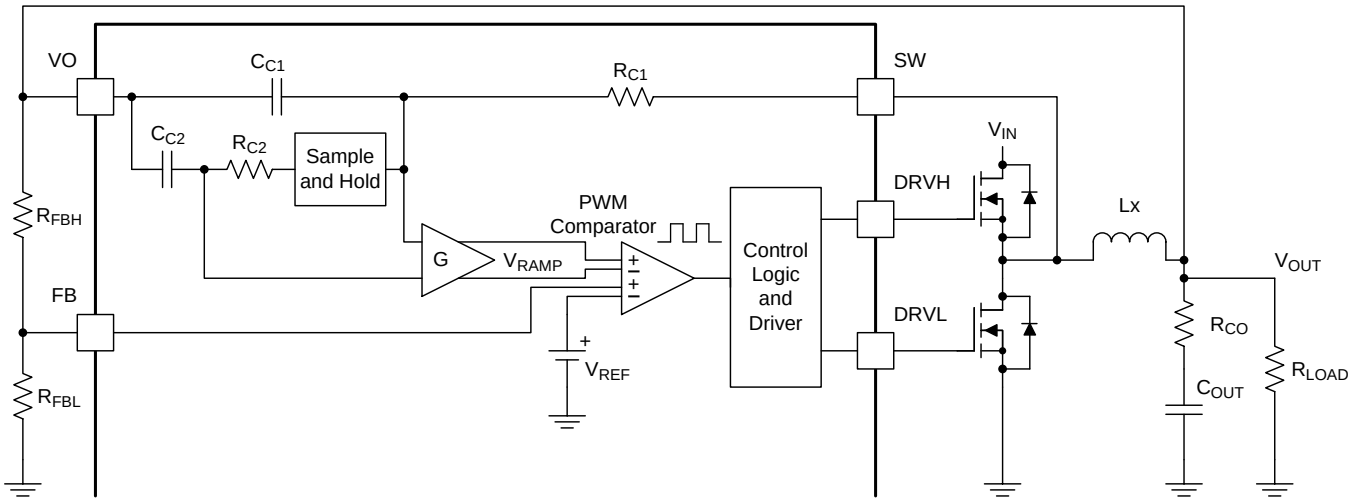


Figure 41. D-CAP3 Mode

The D-CAP3 control architecture includes an internal ripple generation network enabling the use of very low-ESR output capacitors such as multi-layered ceramic capacitors (MLCC). No external current sensing network or voltage compensators are required with D-CAP3 control architecture. The role of the internal ripple generation network is to emulate the ripple component of the inductor current information and then combine it with the voltage feedback signal to regulate the loop operation. For any control topologies supporting no external compensation design, there is a minimum and/or maximum range of the output filter it can support. The output filter used with the TPS53513 is a lowpass L-C circuit. This L-C filter has double pole that is described in Equation 1.

$$f_P = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} \quad (1)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the TPS53513. The low frequency L-C double pole has a 180 degree in phase. At the output filter frequency, the gain rolls off at a –40dB per decade rate and the phase drops rapidly. The internal ripple generation network introduces a high-frequency zero that reduces the gain roll off from –40dB to –20dB per decade and increases the phase to 90 degree one decade above the zero frequency.

The inductor and capacitor selected for the output filter must be such that the double pole of Equation 1 is located close enough to the high-frequency zero so that the phase boost provided by the high-frequency zero provides adequate phase margin for the stability requirement.

Table 1. Locating the Zero

SWITCHING FREQUENCIES (f_{SW}) (kHz)	ZERO (f_Z) LOCATION (kHz)
250 and 300	6
400 and 500	7
600 and 750	9
850 and 1000	12

After identifying the application requirements, the output inductance should be designed so that the inductor peak-to-peak ripple current is approximately between 25% and 35% of the $I_{CC(max)}$ (peak current in the application). Use Table 1 to help locate the internal zero based on the selected switching frequency. In general, where reasonable (or smaller) output capacitance is desired, Equation 2 can be used to determine the necessary output capacitance for stable operation.

$$f_P = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} = f_Z \quad (2)$$

If MLCC is used, consider the derating characteristics to determine the final output capacitance for the design. For example, when using an MLCC with specifications of 10-µF, X5R and 6.3 V, the deratings by DC bias and AC bias are 80% and 50% respectively. The effective derating is the product of these two factors, which in this case is 40% and 4-µF. Consult with capacitor manufacturers for specific characteristics of the capacitors to be used in the system/applications.

Table 2 shows the recommended output filter range for an application design with the following specifications:

- Input voltage, V_{IN} = 12 V
- Switching frequency, f_{SW} = 600 kHz
- Output current, I_{OUT} = 8 A

The minimum output capacitance is verified by the small signal measurement conducted on the EVM using the following two criteria:

- Loop crossover frequency is less than one-half the switching frequency (300 kHz)
- Phase margin at the loop crossover is greater than 50 degrees

For the maximum output capacitance recommendation, simplify the procedure to adopt an unrealistically high output capacitance for this type of converter design, then verify the small signal response on the EVM using the following one criteria:

- Phase margin at the loop crossover is greater than 50 degrees

As indicated by the phase margin, the actual maximum output capacitance ($C_{OUT(max)}$) can continue to go higher. However, small signal measurement (bode plot) should be done to confirm the design.

Select a MODE pin configuration as shown in Table 3 to double the R-C time constant option for the maximum output capacitance design and application. Select a MODE pin configuration to use single R-C time constant option for the normal (or smaller) output capacitance design and application.

The MODE pin also selects SKIP-mode or FCCM-mode operation.

Table 2. Recommended Component Values

V_{OUT} (V)	R_{LOWER} (kΩ)	R_{UPPER} (kΩ)	L_{OUT} (µH)	$C_{OUT(min)}$ (µF) (1)	CROSS-OVER (kHz)	PHASE MARGIN (°)	$C_{OUT(max)}$ (µF) (1)	INTERNAL RC SETTING (µs)	INDUCTOR $\Delta I/I_{CC(max)}$	$I_{CC(max)}$ (A)
0.6	10	0	0.36 PIMB065T-R36MS	3 × 100	247	70		40	33%	8
					48	62	30 x 100	80		
1.2		10	0.68 PIMB065T-R68MS	9 × 22	207	53		40	33%	
					25	84	30 x 100	80		
2.5		31.6	1.2 PIMB065T-1R2MS	4 × 22	185	57		40	34%	
					11	63	30 x 100	80		
3.3		45.3	1.5 PIMB065T-1R5MS	3 × 22	185	57		40	33%	
					9	59	30 x 100	80		
5.5		82.5	2.2 PIMB065T-2R2MS	2 × 22	185	51		40	28%	
					7	58	30 x 100	80		

(1) All $C_{OUT(min)}$ and $C_{OUT(max)}$ capacitor specifications are 1206, X5R, 10 V.

For higher output voltage at or above 2.0 V, additional phase boost might be required in order to secure sufficient phase margin due to phase delay/loss for higher output voltage (large on-time (t_{ON})) setting in a fixed on time topology based operation.

A feedforward capacitor placing in parallel with R_{UPPER} is found to be very effective to boost the phase margin at loop crossover. Refer to TI application note SLVA289 for details.

Table 3. Mode Selection and Internal RAMP RC Time Constant

MODE SELECTION	ACTION	R_{MODE} (kΩ)	R-C TIME CONSTANT (µs)	SWITCHING FREQUENCIES f_{SW} (kHz)
Skip Mode	Pull down to GND	0	60	275 and 325
			50	425 and 525
			40	625 and 750
			30	850 and 1000
		150	120	275 and 325
			100	425 and 525
			80	625 and 750
			60	850 and 1000
FCCM(1)	Connect to PGOOD	20	60	275 and 325
			50	425 and 525
			40	625 and 750
			30	850 and 1000
		150	120	275 and 325
			100	425 and 525
			80	625 and 750
			60	850 and 1000
FCCM	Connect to VREG	0	120	275 and 325
			100	425 and 525
			80	625 and 750
			60	850 and 1000

(1) Device goes into Forced CCM (FCCM) after PGOOD becomes high.

Sample and Hold Circuitry

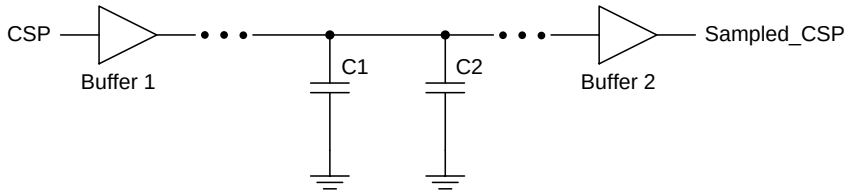


Figure 42. Sample and Hold Circuitry (Patent Pending)

The sample and hold circuitry is the difference between D-CAP3 and D-CAP2. The sample and hold circuitry, which is an advance control scheme to boost output voltage accuracy higher on the TPS53915, is one of features of the TPS53915. The sample and hold circuitry generates a new DC voltage of CSN instead of the voltage which is produced by R_{C2} and C_{C2} which allows for tight output-voltage accuracy and makes the TPS53915 more competitive.

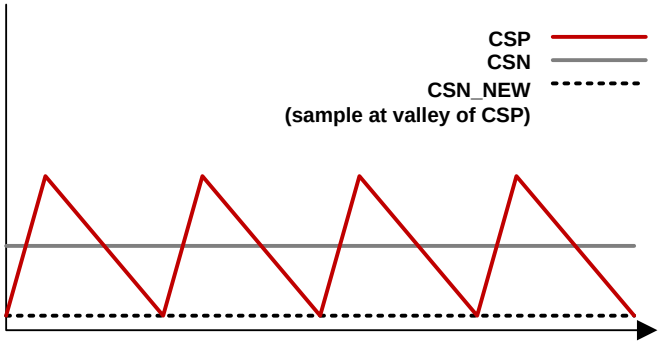


Figure 43. Continuous Conduction Mode (CCM) With Sample and Hold Circuitry

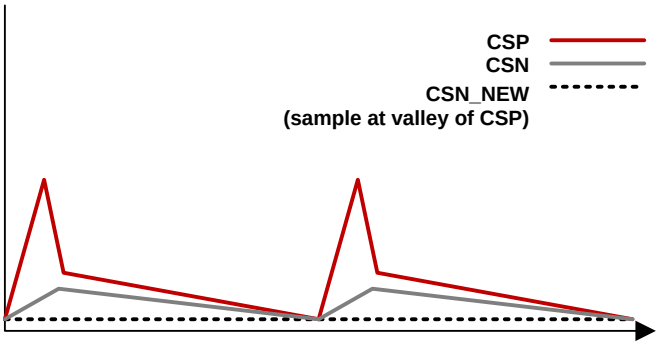


Figure 44. Discontinuous Conduction Mode (DCM) With Sample and Hold Circuitry

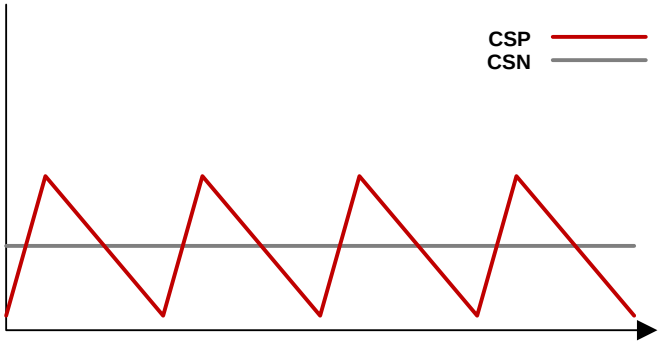


Figure 45. Continuous Conduction Mode (CCM) Without Sample and Hold Circuitry

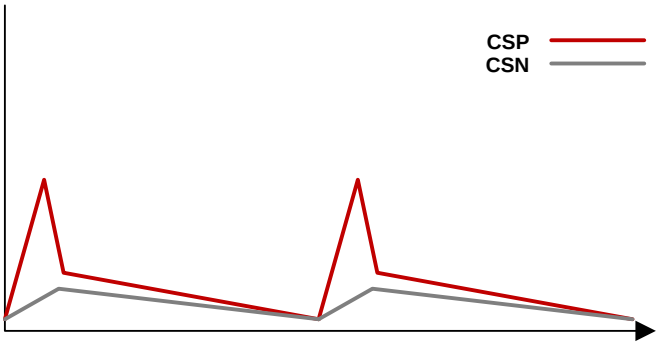


Figure 46. Discontinuous Conduction Mode (DCM) Without Sample and Hold Circuitry

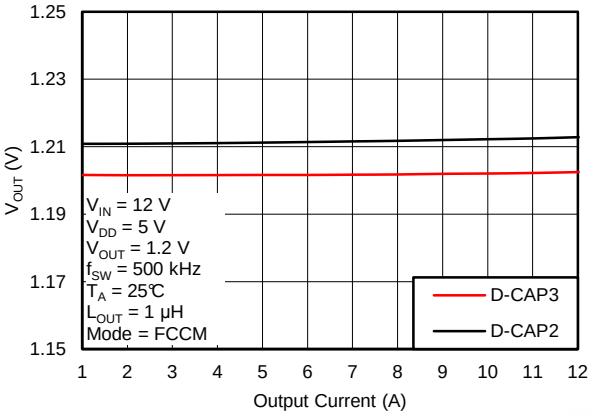


Figure 47. Output Voltage vs Output Current

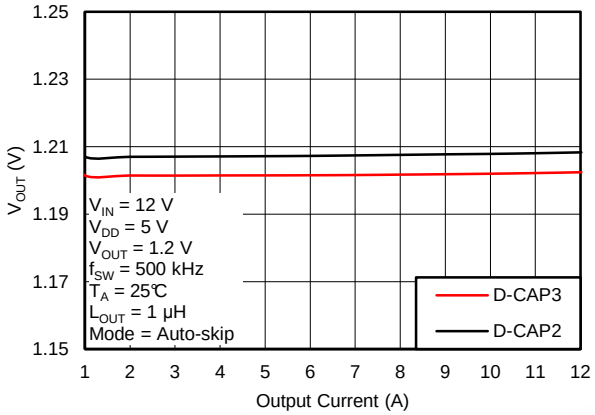


Figure 48. Output Voltage vs Output Current

Auto-Skip Eco-mode™ Light Load Operation

While the MODE pin is pulled to GND directly or via 150-kΩ resistor, the TPS53915 automatically reduces the switching frequency at light-load conditions to maintain high efficiency. This section describes the operation in detail.

As the output current decreases from heavy load condition, the inductor current also decreases until the rippled valley of the inductor current touches zero level. Zero level is the boundary between the continuous-conduction and discontinuous-conduction modes. The synchronous MOSFET turns off when this zero inductor current is detected. As the load current decreases further, the converter runs into discontinuous-conduction mode (DCM). The on-time is maintained to a level approximately the same as during continuous-conduction mode operation so that discharging the output capacitor with a smaller load current to the level of the reference voltage requires more time. The transition point to the light-load operation $I_{O(LL)}$ (for example: the threshold between continuous- and discontinuous-conduction mode) is calculated as shown in Equation 3.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (3)$$

where

- f_{SW} is the PWM switching frequency

Using only ceramic capacitors is recommended for Auto-skip mode.

Adaptive Zero-Crossing

The TPS53915 uses an adaptive zero-crossing circuit to perform optimization of the zero inductor-current detection during skip-mode operation. This function allows ideal low-side MOSFET turn-off timing. The function also compensates the inherent offset voltage of the Z-C comparator and delay time of the Z-C detection circuit. Adaptive zero-crossing prevents SW-node swing-up caused by too-late detection and minimizes diode conduction period caused by too-early detection. As a result, the device delivers better light-load efficiency.

Forced Continuous-Conduction Mode

When the MODE pin is tied to the PGOOD pin through a resistor, the controller operates in continuous conduction mode (CCM) during light-load conditions. During CCM, the switching frequency maintained to an amost constant level over the entire load range which is suitable for applications requiring tight control of the switching frequency at the cost of lower efficiency.

Power-Good

The TPS53915 has power-good output that indicates high when switcher output is within the target. The power-good function is activated after the soft-start operation is complete. If the output voltage becomes within ±8% of the target value, internal comparators detect the power-good state and the power-good signal becomes high after a 1-ms internal delay. If the output voltage goes outside of ±16% of the target value, the power-good signal becomes low after a 2-µs internal delay. The power-good output is an open-drain output and must be pulled-up externally.

Current Sense and Overcurrent Protection

The TPS53915 has cycle-by-cycle overcurrent limiting control. The inductor current is monitored during the OFF state and the controller maintains the OFF state during the period that the inductor current is larger than the overcurrent trip level. In order to provide good accuracy and a cost-effective solution, the TPS53915 supports temperature compensated MOSFET $R_{DS(on)}$ sensing. Connect the TRIP pin to GND through the trip-voltage setting resistor, R_{TRIP}. The TRIP terminal sources I_{TRIP} current, which is 10 µA typically at room temperature, and the trip level is set to the OCL trip voltage V_{TRIP} as shown in Equation 4.

$$V_{TRIP} = R_{TRIP} \times I_{TRIP}$$

where

- V_{TRIP} is in mV
- R_{TRIP} is in kΩ
- I_{TRIP} is in µA (4)

The inductor current is monitored by the voltage between the GND pin and SW pin so that the SW pin is properly connected to the drain terminal of the low-side MOSFET. I_{TRIP} has a 3000-ppm/°C temperature slope to compensate the temperature dependency of $R_{DS(on)}$. The GND pin acts as the positive current-sensing node. Connect the GND pin to the proper current sensing device, (for example, the source terminal of the low-side MOSFET.)

Because the comparison occurs during the OFF state, V_{TRIP} sets the valley level of the inductor current. Thus, the load current at the overcurrent threshold, I_{OCP}, is calculated as shown in Equation 5.

$$I_{OCP} = \frac{V_{TRIP}}{\left(8 \times R_{DS(on)}\right)} + \frac{I_{IND(ripple)}}{2} = \frac{V_{TRIP}}{\left(8 \times R_{DS(on)L}\right)} + \frac{1}{2 \times L \times f_{SW}} \times \frac{\left(V_{IN} - V_{OUT}\right) \times V_{OUT}}{V_{IN}}$$

where

- $R_{DS(on)}$ is the on-resistance of the low-side MOSFET
- R_{TRIP} is in kΩ (5)

In an overcurrent condition, the current to the load exceeds the current to the output capacitor thus the output voltage tends to decrease. Eventually, the output voltage crosses the undervoltage-protection threshold and shuts down.

Overvoltage and Undervoltage Protection

The TPS53915 monitors a resistor-divided feedback voltage to detect overvoltage and undervoltage. When the feedback voltage becomes lower than 68% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins counting. After 1 ms, the TPS53915 latches OFF both high-side and low-side MOSFETs drivers. The UVP function enables after soft-start is complete.

When the feedback voltage becomes higher than 120% of the target voltage, the OVP comparator output goes high and the circuit latches OFF the high-side MOSFET driver and turns on the low-side MOSFET until reaching a negative current limit. Upon reaching the negative current limit, the low-side FET is turned off and the high-side FET is turned on again for a minimum on-time. The TPS53915 operates in this cycle until the output voltage is pulled down under the UVP threshold voltage for 1 ms. After the 1-ms UVP delay time, the high-side FET is latched off and low-side FET is latched on. The fault is cleared with a reset of VDD or by re-toggling EN pin.

Out-Of-Bounds Operation (OOB)

The TPS53915 has an out-of-bounds (OOB) overvoltage protection that protects the output load at a much lower overvoltage threshold of 8% above the target voltage. OOB protection does not trigger an overvoltage fault, so the device is not latched off after an OOB event. OOB protection operates as an early no-fault overvoltage-protection mechanism. During the OOB operation, the controller operates in forced PWM mode only by turning on the low-side FET. Turning on the low-side FET beyond the zero inductor current quickly discharges the output capacitor thus causing the output voltage to fall quickly towards the setpoint. During the operation, the cycle-by-cycle negative current limit is also activated to ensure the safe operation of the internal FETs.

UVLO Protection

The TPS53915 monitors the voltage on the VDD pin. If the VDD pin voltage is lower than the UVLO off-threshold voltage, the switch mode power supply shuts off. If the VDD voltage increases beyond the UVLO on-threshold voltage, the controller turns back on. UVLO is a non-latch protection.

Thermal Shutdown

The TPS53915 monitors internal temperature. If the temperature exceeds the threshold value (typically 140°C), TPS53915 shuts off. When the temperature falls approximately 40°C below the threshold value, the device turns on. Thermal shutdown is a non-latch protection.

PMBus GENERAL SPECIFICATIONS

The PMBus General Descriptions

The TPS53915 has seven internal custom user-accessible 8-bit registers. The PMBus interface has been designed for program flexibility, supporting a direct format for write operation. Read operations are supported for both combined format and stop separated format. While there is no auto increment/decrement capability in the The TPS53915 PMBus logic, a tight software loop can be designed to randomly access the next register, regardless of which register was accessed first. The START and STOP commands frame the data packet and the REPEAT START condition is allowed when necessary.

The device can operate in either standard mode (100 kb/s) or fast mode (400 kb/s).

PMBus Slave Address Selection

The seven-bit slave address is $001A_3A_2A_1A_0x$, where $A_3A_2A_1A_0$ is set by the ADDR pin on the device. Bit 0 is the data direction bit, i.e., $001A_3A_2A_1A_00$ is used for write operation and $001A_3A_2A_1A_01$ is used for read operation.

PMBus Address Selection

The TPS53915 allows up to 16 different chip addresses for PMBus communication, with the first three bits fixed as 001. The address selection process is defined by the resistor divider ratio from VREG pin to ADDR pin, and the address detection circuit starts to work only after VDD input supply has risen above its UVLO threshold. The table below lists the divider ratio and some example resistor values. The 1% tolerance resistors with typical temperature coefficient of ±100 ppm/°C are recommended. Higher performance resistors can be used if tighter noise margin is required for more reliable address detection, as shown in Table 4.

Table 4. PMBus Address Selection Settings

PMBus ADDRESS	RESISTOR DIVIDER RATIO (Ω)			(R_{HIGH}) (kΩ) HIGH-SIDE RESISTOR	(R_{LOW}) (kΩ) LOW-SIDE RESISTOR
	($R_{LOW}/R_{LOW}+R_{HIGH}$)	MIN	MAX		
0011111	> 0.557			1	300
0011110	0.5100	0.4958	0.5247	160	165
0011101	0.4625	04482	0.4772	180	154
0011100	0.4182	0.4073	0.4294	200	143
0011011	0.3772	0.3662	0.3886	200	120
0011010	0.3361	0.3249	0.3476	220	110
0011001	0.2985	0.2905	0.3067	249	105
0011000	0.2641	0.2560	0.2725	249	88.7
0010111	0.2298	0.2215	0.2385	240	71.5
0010110	0.1955	0.1870	0.2044	249	60.4
0010101	0.1611	0.1524	0.1703	249	47.5
0010100	0.1268	0.1179	0.1363	249	36.0
0010011	0.0960	0.0900	0.1024	255	27.0
0010010	0.0684	0.0622	0.0752	255	18.7
0010001	0.0404	0.0340	0.0480	270	11.5
0010000	< 0.013			300	1

Supported Formats

The supported formats are described in this section.

Direct Format: Write

The simplest format for a PMBus write is direct format. After the START condition [S], the slave chip address is sent, followed by an eighth bit indicating a write. The TPS53915 then acknowledges that it is being addressed, and the master responds with an 8-bit register address byte. The slave acknowledges and the master sends the appropriate 8-bit data byte. Again the slave acknowledges and the master terminates the transfer with the STOP condition [P].

Combined Format: Read

After the START condition [S], the slave chip address is sent, followed by an eighth bit indicating a write. The TPS53915 then acknowledges that it is being addressed, and the master responds with an 8-bit register address byte. The slave acknowledges and the master sends the repeated START condition [Sr]. Again the slave chip address is sent, followed by an eighth bit indicating a read. The slave responds with an acknowledge followed by previously addressed 8 bit data byte. The master then sends a non-acknowledge (NACK) and finally terminates the transfer with the STOP condition [P].

Stop-Separated Reads

Stop-separated read features are also available. This format allows a master to initialize the register address pointer for a read and return to that slave at a later time to read the data. In this format the slave chip address followed by a write bit are sent after a START [S] condition. The TPS53915 then acknowledges it is being addressed, and the master responds with the 8-bit register address byte. The master then sends a STOP or RESTART condition and may then address another slave. After performing other tasks, the master can send a START or RESTART condition to the device with a read command. The device acknowledges this request and returns the data from the register location that had been set up previously.

Supported PMBus Commands

The TPS53915 supports the PMBus commands shown in Table 5 only. Not all features of each PMBus command are supported. The CLEAR_FAULTS, STORE_DEFAULT_ALL and RESTORE_DEFAULT_ALL commands have no data bytes. The non-volatile memory (NVM) cells inside the TPS53915 can permanently store some registers.

Table 5. Supported PMBus Commands

COMMAND	NOTES
OPERATION	Turn on or turn off switching converter only
ON_OFF_CONFIG	ON/OFF configuration
CLEAR_FAULTS	Clear all latched status flags
WRITE_PROTECT	Control writing to the PMBus device
STORE_DEFAULT_ALL	Store contents of user-accessible registers to non-volatile memory cells
RESTORE_DEFAULT_ALL	Copy contents of non-volatile memory cells to user-accessible registers
STATUS_WORD	PMBus read-only status and flag bits
CUSTOM_REG	MFR_SPECIFIC_00 (Custom Register 0): Custom register
DELAY_CONTROL	MFR_SPECIFIC_01 (Custom Register 1): Power on and power good delay times
MODE_SOFT_START_CONFIG	MFR_SPECIFIC_02 (Custom Register 2): Mode and soft-start time
FREQUENCY_CONFIG	MFR_SPECIFIC_03 (Custom Register 3): Switching frequency control
VOUT_ADJUSTMENT	MFR_SPECIFIC_04 (Custom Register 4): Output voltage adjustment control
VOUT_MARGIN	MFR_SPECIFIC_05 (Custom Register 5): Output voltage margin levels
UVLO_THRESHOLD	MFR_SPECIFIC_06 (Custom Register 6): Turn-on input voltage UVLO threshold

Unsupported PMBus Commands

Do not send any unsupported commands to the TPS53915. Even though the device receives an unsupported commands, it can acknowledge the unsupported commands and any related data bytes by properly sending the ACK bits. However, the device ignores the unsupported commands and any related data bytes, which means they do not affect the device operation in any way. Although the TPS53915 may acknowledge but ignore unsupported commands and data bytes, it can however, set the CML bit in the STATUS_BYTE register and then pull down the ALERT pin to notify the host. For this reason, unsupported commands and data bytes should not be sent to TPS53915.

OPERATION [01h] (R/W Byte)

The TPS53915 supports only the functions of the OPERATION command shown in Table 6.

Table 6. OPERATION Command Supported Functions

COMMAND	DEFINITION	DESCRIPTION	NVM
OPERATION<7>	ON_OFF	0: turn off switching converter 1: turn on switching converter	—
OPERATION<6>	—	not supported and don't care	—
OPERATION<5:2>	OPMARGIN<3:0>	00xx: turn off output voltage margin function 0101: turn on output voltage margin low and ignore fault 0110: turn on output voltage margin low and act on fault 1001: turn on output voltage margin high and ignore fault 1010: turn on output voltage margin high and act on fault	—
OPERATION<1>	—	not supported and don't care	—
OPERATION<0>	—	not supported and don't care	—

ON_OFF_CONFIG [02h] (R/W Byte)

The TPS53915 supports only the functions of the ON_OFF_CONFIG command shown in Table 7.

Table 7. ON_OFF_CONFIG Command Supported Functions

COMMAND	DEFINITION	DESCRIPTION	NVM
ON_OFF_CONFIG<7>	—	not supported and don't care	—
ON_OFF_CONFIG<6>	—	not supported and don't care	—
ON_OFF_CONFIG<5>	—	not supported and don't care	—
ON_OFF_CONFIG<4>	PU	not supported and always set to 1	—
ON_OFF_CONFIG<3>	CMD	0: ignore ON_OFF bit (OPERATION<7>)(1) 1: act on ON_OFF bit (OPERATION<7>)	Yes
ON_OFF_CONFIG<2>	CP	0: ignore EN pin 1: act on EN pin(1)	Yes
ON_OFF_CONFIG<1>	PL	not supported and always set to 1	—
ON_OFF_CONFIG<0>	SP	not supported and always set to 1	—

(1) TI default.

Conditions required to enable the switcher:

- If CMD is cleared and CP is set, then the switcher can be enabled only by the EN pin.
- If CMD is set and CP is cleared, then the switcher can be enabled only by the ON_OFF bit (OPERATION<7>) via PMBus.
- If both CMD and CP are set, then the switcher can be enabled only when both the ON_OFF bit (OPERATION<7>) and the EN pin are commanding to enable the device.
- If both CMD and CP are cleared, then the switcher is automatically enabled after the ADDR detection sequence completes, regardless of EN pin and ON_OFF bit polarities.

WRITE_PROTECT [10h] (R/W Byte)

The WRITE PROTECT command is used to control writing to the PMBus device. The intent of this command is to provide protection against accidental changes. This command has one data byte as described in Table 8.

Table 8. WRITE_PROTECT Command Supported Functions

COMMAND	DEFINITION	DESCRIPTION		NVM
WRITE_PROTECT<7:0>	WP<7:0>	10000000:	Disable all writes, except the WRITE_PROTECT command.	—
		01000000:	Disable all writes, except the WRITE_PROTECT and OPERATION commands.	—
		00100000:	Disable all writes, except the WRITE_PROTECT, OPERATION, and ON_OFF_CONFIG commands.	—
		00000000:	Enable writes to all commands.	—
		Others:	Fault data	—

CLEAR_FAULTS [03h] (Send Byte)

The CLEAR_FAULTS command is used to clear any fault bits in the STATUS_WORD and STATUS_BYTE registers that have been set. This command clears all bits in all status registers. Simultaneously, the TPS53915 releases its ALERT signal output if the device is asserting the ALERT signal. If the FAULT condition is still present when the bit is cleared, the fault bits shall immediately be set again, and the ALERT signal should also be re-asserted.

The CLEAR_FAULTS does not cause a unit that has latched off for a FAULT condition to restart. Units that have been shut down for a FAULT condition can be restarted with one of the following conditions.

- The output is commanded through the EN pin and/or ON_OFF bit based on the ON_OFF_CONFIG setting to turn off and then to turn back on.
- VDD power is cycled for TPS53915

The CLEAR_FAULT command is used to clear the fault bits in the STATUS_WORD and STATUS_BYTE commands, and to release the ALERT pin. It is recommended not to send CLEAR_FAULT command when there is no fault to cause the ALERT pin to pull down.

STORE_DEFAULT_ALL [11h] (Send Byte)

The STORE_DEFAULT_ALL command instructs TPS53915 to copy the entire contents of the operating memory to the corresponding locations in the NVM. The updated contents in the non-volitile memory (NVM)s become the new default values. The STORE_DEFAULT_ALL command can be used while the device is operating. However, the device may be unresponsive during the copy operation with unpredictable results. (see *PMBus Power System Management Protocol Specificaiton*, Part II - Command Language, Revision, 1.2, 6 Sept. 2010. www.powerSIG.org). It is recommended not to exceed 1000 write/erase cycles for non-volatile memory (NVM).

RESTORE_DEFAULT_ALL [12h] (Send Byte)

The RESTORE_DEFAULT_ALL command instructs TPS53915 to copy the entire contents of the NVMs to the corresponding locations in the operating memory. The values in the operating memory are overwritten by the value retrieved from the NVM. It is permitted to use the RESTORE_DEFAULT_ALL command while the device is operating. However, the device may be unresponsive during the copy operation with unpredictable results.

STATUS_WORD [79h] (Read Word)

The TPS53915 does not support all functions of the STATUS_WORD command. A list of supported functions appears in Table 9. A status bit reflects the current state of the converter. Status bit becomes high when the specified condition has occurred and goes low when the specified condition has disappeared. A flag bit is a latched bit that becomes high when the specified condition has occurred and does not go back low when the specified condition has disappeared. STATUS_BYTE command is a subset of the STATUS_WORD command, or more specifically the lower byte of the STATUS_WORD.

Table 9. STATUS_WORD Command Supported Functions

COMMAND	DEFINITION	DESCRIPTION
Low Byte: STATUS_BYTE [78h]		
Low STATUS_WORD<7>	BUSY	not supported and always set to 0
Low STATUS_WORD<6>	OFF	0: raw status indicating device is providing power to output voltage 1: raw status indicating device is not providing power to output voltage
Low STATUS_WORD<5>	VOUT_OV	0: latched flag indicating no output voltage overvoltage fault has occurred 1: latched flag indicating an output voltage overvoltage fault has occurred
Low STATUS_WORD<4>	IOUT_OC	0: latched flag indicating no output current overcurrent fault has occurred 1: latched flag indicating an output current overcurrent fault has occurred
Low STATUS_WORD<3>	VIN_UV	0: latched flag indicating input voltage is above the UVLO turn-on threshold 1: latched flag indicating input voltage is below the UVLO turn-on threshold
Low STATUS_WORD<2>	TEMP	0: latched flag indicating no OT fault has occurred 1: latched flag indicating an OT fault has occurred
Low STATUS_WORD<1>	CML	0: latched flag indicating no communication, memory or logic fault has occurred 1: latched flag indicating a communication, memory or logic fault has occurred
Low STATUS_WORD<0>	OTHER	not supported and always set to 0
High Byte		
High STATUS_WORD<7>	VOUT	0: latched flag indicating no output voltage fault or warning has occurred 1: latched flag indicating a output voltage fault or warning has occurred
High STATUS_WORD<6>	IOUT	0: latched flag indicating no output current fault or warning has occurred 1: latched flag indicating an output current fault or warning has occurred
High STATUS_WORD<5>	INPUT	0: latched flag indicating no input voltage fault or warning has occurred 1: latched flag indicating a input voltage fault or warning has occurred
High STATUS_WORD<4>	MFR	not supported and always set to 0
High STATUS_WORD<3>	$\overline{\text{PGOOD}}$	0: raw status indicating PGOOD pin is at logic high 1: raw status indicating PGOOD pin is at logic low
High STATUS_WORD<2>	FANS	not supported and always set to 0
High STATUS_WORD<1>	OTHER	not supported and always set to 0
High STATUS_WORD<0>	UNKNOWN	not supported and always set to 0

The latched flags of faults can be removed or corrected only until **one** of the following conditions occurs:

- The device receives a CLEAR_FAULTS command.
- The output is commanded through the EN pin and/or ON_OFF bit based on the ON_OFF_CONFIG setting to turn off and then to turn back on
- VDD power is cycled for TPS53915

If the FAULT condition remains present when the bit is cleared, the fault bits are immediately set again, and the $\overline{\text{ALERT}}$ signal is re-asserted.

TPS53915 supports the $\overline{\text{ALERT}}$ pin to notify the host of FAULT conditions. Therefore, the best practice for monitoring the fault conditions from the host is to treat the $\overline{\text{ALERT}}$ pin as an interrupt source for triggering the corresponding interrupt service routine. It is recommended not to keep polling the STATUS_WORD or STATUS_BYTE registers from the host to reduce the firmware overhead of the host.

CUSTOM_REG (MFR_SPECIFIC_00) [D0h] (R/W Byte)

Custom register 0 provides the flexibility for users to store any desired non-volatile information. For example, users can program this register to track versions of implementation or other soft identification information. The details of each setting are listed in Table 10.

Table 10. CUSTOM_REG (MFR_SPECIFIC_00) Settings

COMMAND	DEFINITION	DESCRIPTION	NVM
CUSTOM_REG<7>	—	not supported and don't care	—
CUSTOM_REG<6>	—	not supported and don't care	—
CUSTOM_REG<5:0>	CUSTOMWORD <5:0>	00000:(1) can be used to store any desired non-volatile information.	Yes

(1) TI Default

DELAY_CONTROL (MFR_SPECIFIC_01) [D1h] (R/W Byte)

Custom register 1 provides software control over key timing parameters of the controller: Power-on delay (POD) time and power-good delay (PGD) time. The details of each setting are listed in Table 11.

Table 11. DELAY_CONTROL (MFR_SPECIFIC_01) Settings

COMMAND	DEFINITION	DESCRIPTION	NVM
DELAY_CONTROL<7>	—	not supported and don't care	—
DELAY_CONTROL<6>	—	not supported and don't care	—
DELAY_CONTROL<5:3>	PGD<2:0>	000: 256 µs 001: 512 µs 010: 1.024 ms(1) 011: 2.048 ms 100: 4.096 ms 101: 8.192 ms 110: 16.384 ms 111: 131.072 ms	Yes
DELAY_CONTROL<2:0>	POD<2:0>	000: 356 µs 001: 612 µs 010: 1.124 ms(1) 011: 2.148 ms 100: 4.196 ms 101: 8.292 ms 110: 16.484 ms 111: 32.868 ms	Yes

(1) TI Default

MODE_SOFT_START_CONFIG (MFR_SPECIFIC_02) [D2h] (R/W Byte)

Custom register 2 provides software control over mode selection and soft-start time (t_{SS}). The details of each setting are listed in Table 12.

Table 12. MODE_SOFT_START_CONFIG (MFR_SPECIFIC_02) Settings

COMMAND	DEFINITION	DESCRIPTION	NVM
MODE_SOFT_START_CONFIG<7>	—	not supported and don't care	—
MODE_SOFT_START_CONFIG<6>	—	not supported and don't care	—
MODE_SOFT_START_CONFIG<5>	—	not supported and don't care	—
MODE_SOFT_START_CONFIG<4>	—	not supported and don't care	—
MODE_SOFT_START_CONFIG<3:2>	SST<1:0>	00: 1 ms(1) 01: 2 ms 10: 4 ms 11: 8 ms	Yes
MODE_SOFT_START_CONFIG<1>	HICLOFF	0: hiccup after UV(1) Hiccup interval is (8.96 ms + soft-start time × 7) 1: latch-off after UV	Yes
MODE_SOFT_START_CONFIG<0>	CM	0: DCM(1) 1: FCCM	Yes

(1) TI Default

Figure 49 shows the soft-start timing diagram of TPS53915 with the programmable power-on delay time (t_{POD}), soft-start time (t_{SST}), and PGOOD delay time (t_{PGD}). During the soft-start time, the controller remains in discontinuous conduction mode (DCM), and then switches to forced continuous conduction mode (FCCM) at the end of soft-start if CM bit (MODE_SOFT_START_CONFIG<0>) is set.

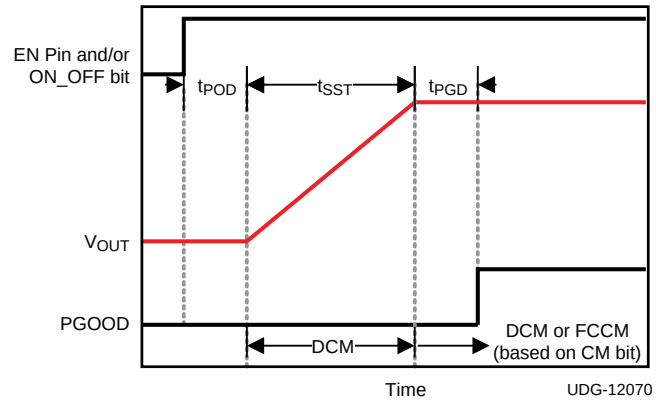


Figure 49. Programmable Soft-Start Timing

FREQUENCY_CONFIG (MFR_SPECIFIC_03) [D3h] (R/W Byte)

Custom register 3 provides software control over frequency setting (FS). The details of FS setting are listed in Table 13.

Table 13. FREQUENCY_CONFIG (MFR_SPECIFIC_03) Settings

COMMAND	DEFINITION	DESCRIPTION	NVM
FREQUENCY_CONFIG<7>	—	not supported and don't care	—
FREQUENCY_CONFIG<6>	—	not supported and don't care	—
FREQUENCY_CONFIG<5>	—	not supported and don't care	—
FREQUENCY_CONFIG<4>	—	not supported and don't care	—
FREQUENCY_CONFIG<3>	—	not supported and don't care	—
FREQUENCY_CONFIG<2:0>	FS<2:0>	000: 250 kHz 001: 300 kHz 010: 400 kHz (1) 011: 500 kHz 100: 600 kHz 101: 750 kHz 110: 850 kHz 111: 1 MHz	Yes

(1) TI default.

VOUT_ADJUSTMENT (MFR_SPECIFIC_04) [D4h] (R/W Byte)

Custom register 4 provides ouput voltage adjustment (VOA) in ±0.75% steps, with a total range of ±9%. When fine adjustment is used together with the margin setting, the change in the output voltage is determined by the multiplication of the two settings.

Table 14. VOUT_ADJUSTMENT (MFR_SPECIFIC_04) Settings

COMMAND	DEFINITION	DESCRIPTION	NVM
VOUT_ADJUSTMENT<7>	—	not supported and don't care	—
VOUT_ADJUSTMENT<6>	—	not supported and don't care	—
VOUT_ADJUSTMENT<5>	—	not supported and don't care	—
VOUT_ADJUSTMENT<4:0>	VOA<4:0>	111xx: +9.00% 11011: +8.25% 11010: +7.50% 11001: +6.75% 11000: +6.00% 10111: +5.25% 10110: +4.50% 10101: +3.75% 10100: +3.00% 10011: +2.25% 10010: +1.50% 10001: +0.75% 10000: +0%(1) 01111: –0% 01110: –0.75% 01101: –1.50% 01100: –2.25% 01011: –3.00% 01010: –3.75% 01001: –4.50% 01000: –5.25% 00111: –6.00% 00110: –6.75% 00101: –7.50% 00100: –8.25% 000xx: –9.00%	Yes

(1) TI default.

Output Voltage Fine Adjustment Soft Slew Rate

To prevent sudden buildup of voltage across inductor, output voltage fine adjustment setting cannot change output voltage instantaneously. The internal reference voltage must slew slowly to its final target, and SST<1:0> is used to provide further programmability. The details of output voltage fine adjustment slew rate are shown in Table 15.

Table 15. Output Voltage Fine Adjustment Soft Slew Rate Settings

COMMAND	DEFINITION	DESCRIPTION	NVM
MODE_SOFT_START_CONFIG<3:2>	SST<1:0>	00: 1 step per 4 µs(1) 01: 1 step per 8 µs 10: 1 step per 16 µs 11: 1 step per 32 µs	Yes

(1) TI default.

VOUT_MARGIN (MFR_SPECIFIC_05) [D5h] (R/W Byte)

Custom register 5 provides output voltage margin high (VOMH) and output voltage margin low (VOML) settings. This register works in conjunction with PMBus OPERATION command to raise or lower the output voltage by a specified amount. This register settings described in Table 16 are also used together with the fine adjustment setting described in Table 14. For example, setting fine adjustment to +9% and margin to +12% changes the output by +22.08%, whereas setting fine adjustment to –9% and margin to –9% change the output by –17.19%

Table 16. VOUT_MARGIN (MFR_SPECIFIC_05) Settings

COMMAND	DEFINITION	DESCRIPTION	NVM
VOUT_MARGIN<7:4>	VOMH<3:0>	11xx: +12.0% 1011: +10.9% 1010: +9.9% 1001: +8.8% 1000: +7.7% 0111: +6.7% 0110: +5.7% 0101: +4.7%(1) 0100: +3.7% 0011: +2.8% 0010: +1.8% 0001: +0.9% 0000: +0%	Yes
VOUT_MARGIN<3:0>	VOML<3:0>	0000: –0% 0001: –1.1% 0010: –2.1% 0011: –3.2% 0100: –4.2% 0101: –5.2% (1) 0110: –6.2% 0111: –7.1% 1000: –8.1% 1001: –9.0% 1010: –9.9% 1011: –10.7% 11xx: –11.6%	Yes

(1) TI default.

Output Voltage Margin Adjustment Soft-Slew Rate

Similar to the output voltage fine adjustment, margin adjustment also cannot change output voltage instantaneously. The soft-slew rate of margin adjustment is also programmed by SST<1:0>. The details are listed in Table 17.

Table 17. Output Voltage Margin Adjustment Soft-Slew Rate Settings

COMMAND	DEFINITION	DESCRIPTION	NVM
MODE_SOFT_START_CONFIG<3:2>	SST<1:0>	00: 1 step per 4 µs(1) 01: 1 step per 8 µs 10: 1 step per 16 µs 11: 1 step per 32 µs	Yes

(1) TI default.

Figure 50 shows the timing diagram of the output voltage adjustment via PMBus. After receiving the write command of VOUT_ADJUSTMENT (MFR_SPECIFIC_04), the output voltage starts to be adjusted after t_P delay time (about 50 µs). The time duration t_{DAC} for each DAC step change can be controlled by SST bits (MODE_SOFT_START_CONFIG<3:2:> from 4 µs to 32 µs.

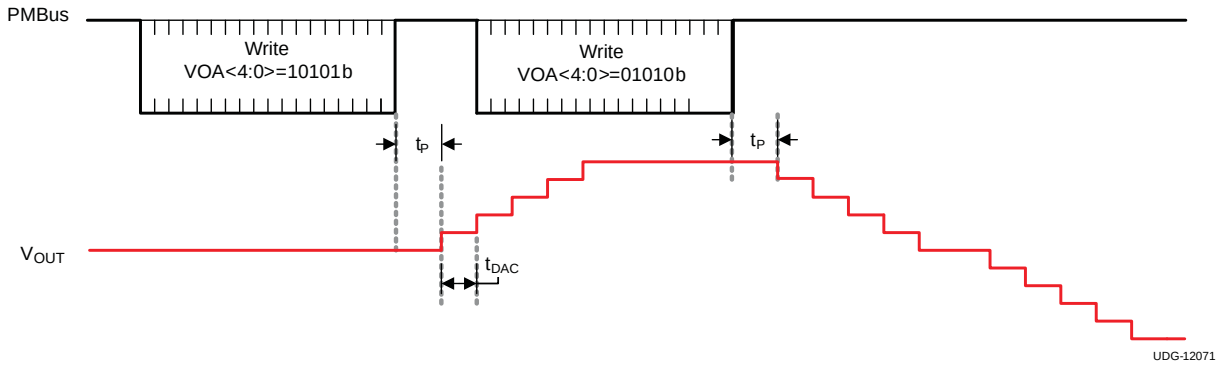


Figure 50. Output Voltage Adjustment via PMBus

The margining function is enabled by setting the OPERATION command, and the margining level is determined by the VOUT_MARGIN (MFR_SPECIFIC_05) command. Figure 51 and Figure 52 illustrate the timing diagrams of the output voltage margining via PMBus. Figure 51 shows setting the margining level first, and then enabling margining by writing OPERATION command. After the OPERATION margin high command enables the margin high setting (VOMH<3:0>), the output voltage starts to be adjusted after t_P delay time (about 50 µs). The time duration t_{DAC} for each DAC step change can be controlled by SST bits (MODE_SOFT_START_CONFIG<3:2>) from 4 µs to 32 µs.

As shown in Figure 52, the margining function is enabled first by a write command of OPERATION. The output voltage starts to be adjusted toward the default margin high level after t_P delay. Since the margining function has been enabled, the output voltage can be adjusted again by sending a different margin high level with a write command of VOUT_MARGIN. The time duration t_{DAC} for each DAC step change can be also controlled by SST bits (MODE_SOFT_START_CONFIG<3:2>) from 4 µs to 32 µs.

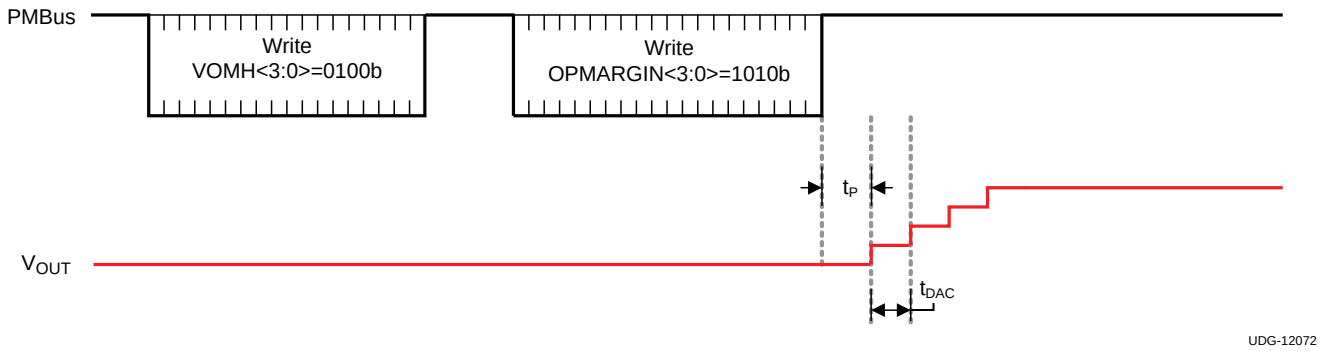


Figure 51. Setting the Margining Level First

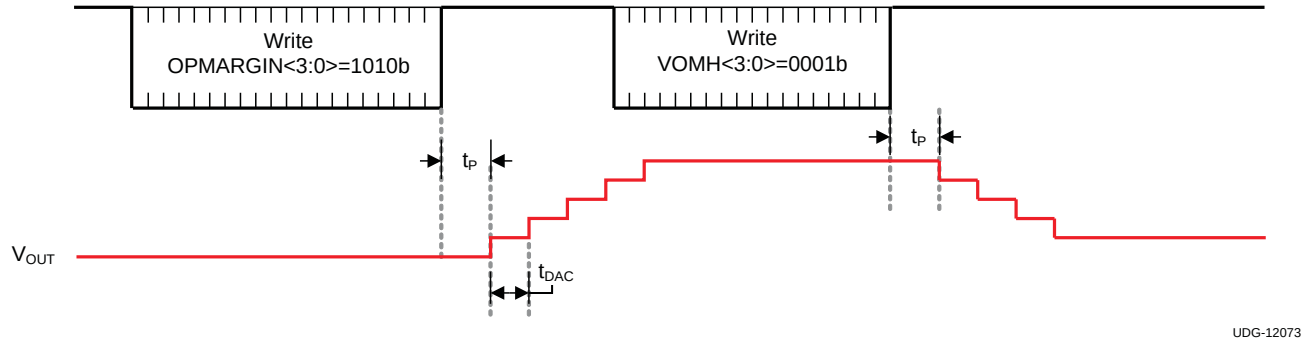


Figure 52. Enabling Margining First

UVLO_THRESHOLD (MFR_SPECIFIC_06) [D6h]

Custom register 6 provides some limited programmability of input supply UVLO threshold, as described in Table 18. The default turn-on UVLO threshold is 4.25 V.

Table 18. UVLO_THRESHOLD (MFR_SPECIFIC_06) Settings

COMMAND	DEFINITION	DESCRIPTION	NVM
UVLO_THRESHOLD<7>	—	not supported and don't care	—
UVLO_THRESHOLD<6>	—	not supported and don't care	—
UVLO_THRESHOLD<5>	—	not supported and don't care	—
UVLO_THRESHOLD<4>	—	not supported and don't care	—
UVLO_THRESHOLD<3>	—	not supported and don't care	—
UVLO_THRESHOLD<2:0>	VDDINUVLO<2:0>	0xx: 10.2 V 100: not supported and should not be used 101: 4.25 V(1) 110: 6.0 V 111: 8.1 V	Yes

(1) TI default.

External Components Selection

The external components selection is a simple process using D-CAP3™ Mode. Select the external components using five easy steps

Step 1. Select The Switching Frequency

The default switching frequency (f_{SW}) is pre-set at 400 kHz. The switching frequency can be changed via PMBus function MFR_SPECIFIC_03 (see Table 13).

Step 2: Select the Operation Mode

Select the operation mode using Table 3.

Step 3: Select the Inductor

Determine the inductance value to set the ripple current at approximately ¼ to ½ of the maximum output current. Larger ripple current increases output ripple voltage, improves S/N ratio, and helps stable operation.

$$L = \frac{1}{I_{IND(ripple)} \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} = \frac{3}{I_{OUT(max)} \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} \quad (6)$$

The inductor requires a low DCR to achieve good efficiency. The inductor also requires enough room above peak inductor current before saturation. The peak inductor current is estimated using Equation 7.

$$I_{IND(peak)} = \frac{V_{TRIP}}{8 \times R_{DS(on)}} + \frac{1}{L \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} \quad (7)$$

Step 4: Select the Output Capacitor

The output capacitor selection is determined by output ripple and transient requirement. When operating in CCM, the output ripple has two components as shown in Equation 8. Equation 9 and Equation 10 define these components.

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)} \quad (8)$$

$$V_{RIPPLE(C)} = \frac{I_{L(ripple)}}{8 \times C_{OUT} \times f_{SW}} \quad (9)$$

$$V_{RIPPLE(ESR)} = I_{L(ripple)} \times ESR \quad (10)$$

Step 5: Determine The Value of R1 and R2

The output voltage is programmed by the voltage-divider resistors, R1 and R2, shown in Figure 1. R1 is connected between the VFB pin and the output, and R2 is connected between the VFB pin and GND. The recommended R2 value is from 1 kΩ to 20 kΩ. Determine R1 using Equation 11.

$$R1 = \frac{V_{OUT} - 0.6}{0.6} \times R2 \quad (11)$$

LAYOUT CONSIDERATIONS

Before beginning a design using the TPS53915, consider the following:

- Place the power components (including input and output capacitors, the inductor, and the TPS53915) on the solder side of the PCB. In order to shield and isolate the small signal traces from noisy power lines, insert and connect at least one inner plane to ground.
- All sensitive analog traces and components such as VFB, PGOOD, TRIP, MODE, and ADDR must be placed away from high-voltage switching nodes such as SW and VBST to avoid coupling. Use internal layers as ground planes and shield the feedback trace from power traces and components.
- Pin 22 (GND pin) must be connected directly to the thermal pad. Connect the thermal pad to the PGND pins and then to the GND plane.
- Place the VIN decoupling capacitors as close to the VIN and PGND pins as possible to minimize the input AC-current loop.
- Place the feedback resistor near the IC to minimize the VFB trace distance.

- Place the frequency-setting resistor (ADDR), OCP-setting resistor (R_{TRIP}) and mode-setting resistor (R_{MODE}) close to the device. Use the common GND via to connect the resistors to the GND plane if applicable.
- Place the VDD and VREG decoupling capacitors as close to the device as possible. Provide GND vias for each decoupling capacitor and ensure the loop is as small as possible.
- The PCB trace is defined as switch node, which connects the SW pins and high-voltage side of the inductor. The switch node should be as short and wide as possible.
- Use separated vias or trace to connect SW node to the snubber, bootstrap capacitor, and ripple-injection resistor. Do not combine these connections.
- Place one more small capacitor (2.2 nF- 0402 size) between the VIN and PGND pins. This capacitor must be placed as close to the IC as possible.
- TI recommends placing a snubber between the SW shape and GND shape for effective ringing reduction. The value of snubber design starts at 3 Ω + 470 pF.
- Consider R,C,Cc network (Ripple injection network) component placement and place the AC coupling capacitor, Cc, close to the device, and R and C close to the power stage.
- See Figure 53 for the layout recommendation.

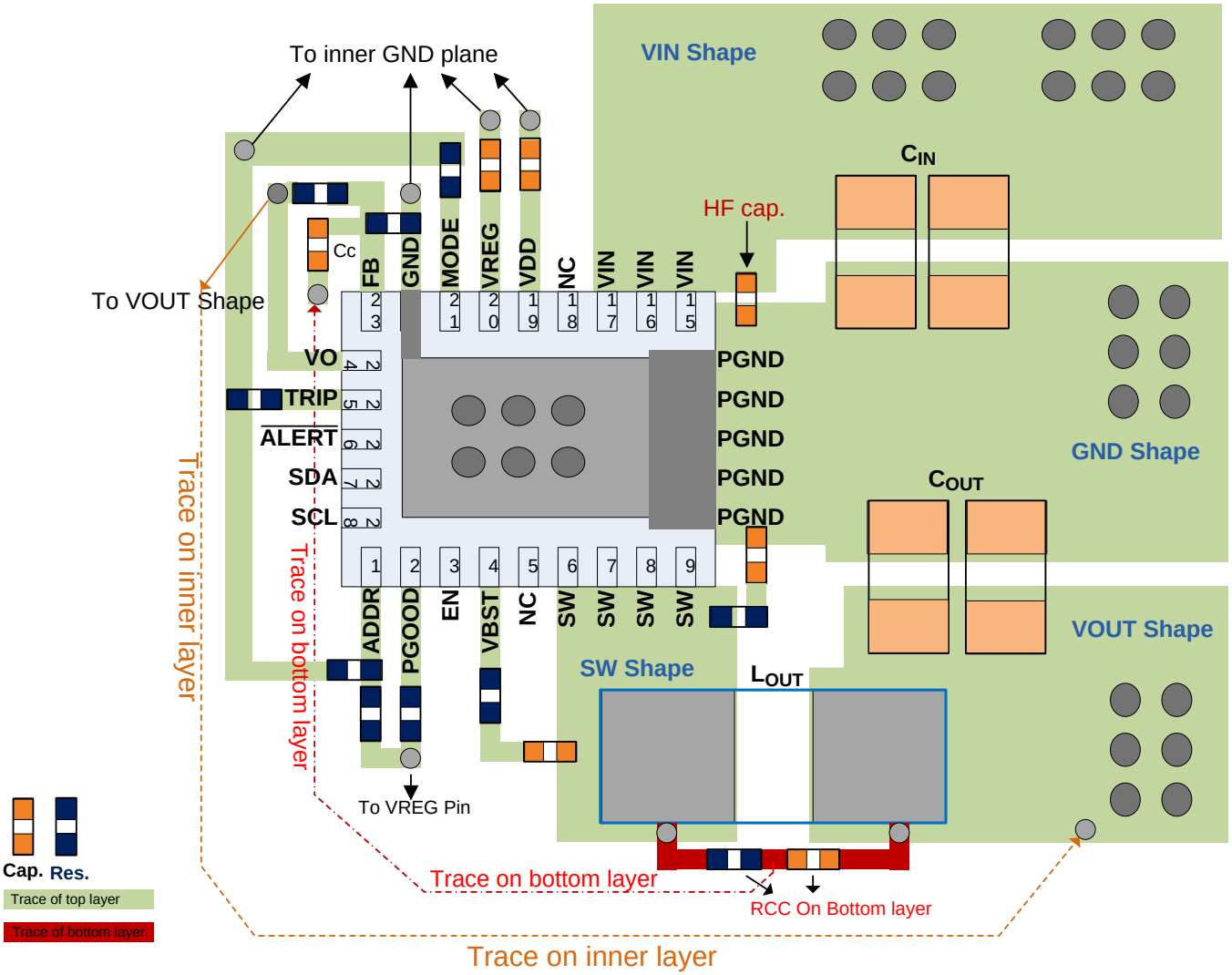


Figure 53. Layout Recommendation

REVISION HISTORY

Changes from Original (November 2013) to Revision A	Page
• Changed device dimensions from 3,5 mm × 4,5 mm to 3.5 mm × 4.5 mm	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS53915RVER	ACTIVE	VQFN	RVE	28	3000	Pb-Free (RoHS Exempt)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS53915	Samples
TPS53915RVET	ACTIVE	VQFN	RVE	28	250	Pb-Free (RoHS Exempt)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS53915	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

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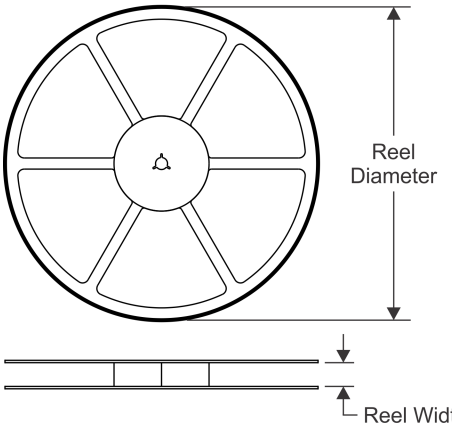
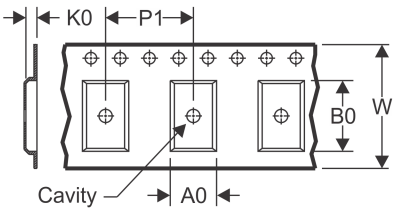
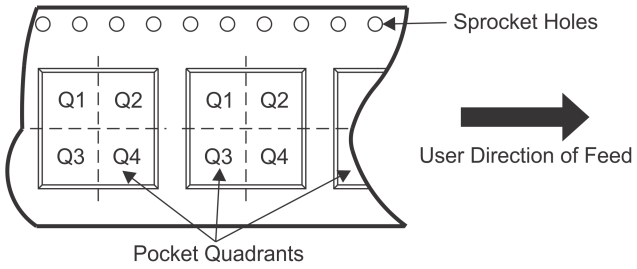


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

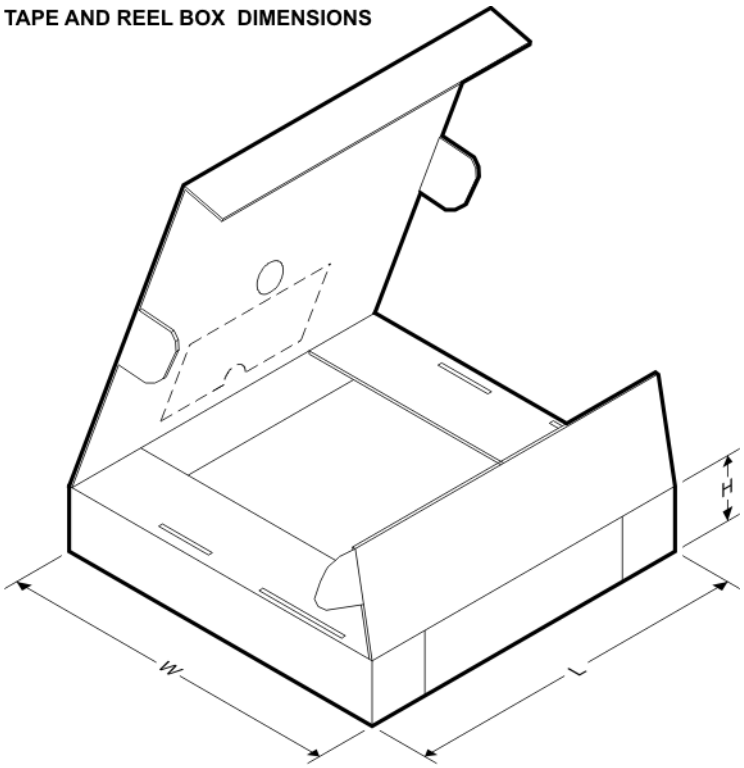
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS53915RVER	VQFN	RVE	28	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
TPS53915RVET	VQFN	RVE	28	250	180.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1

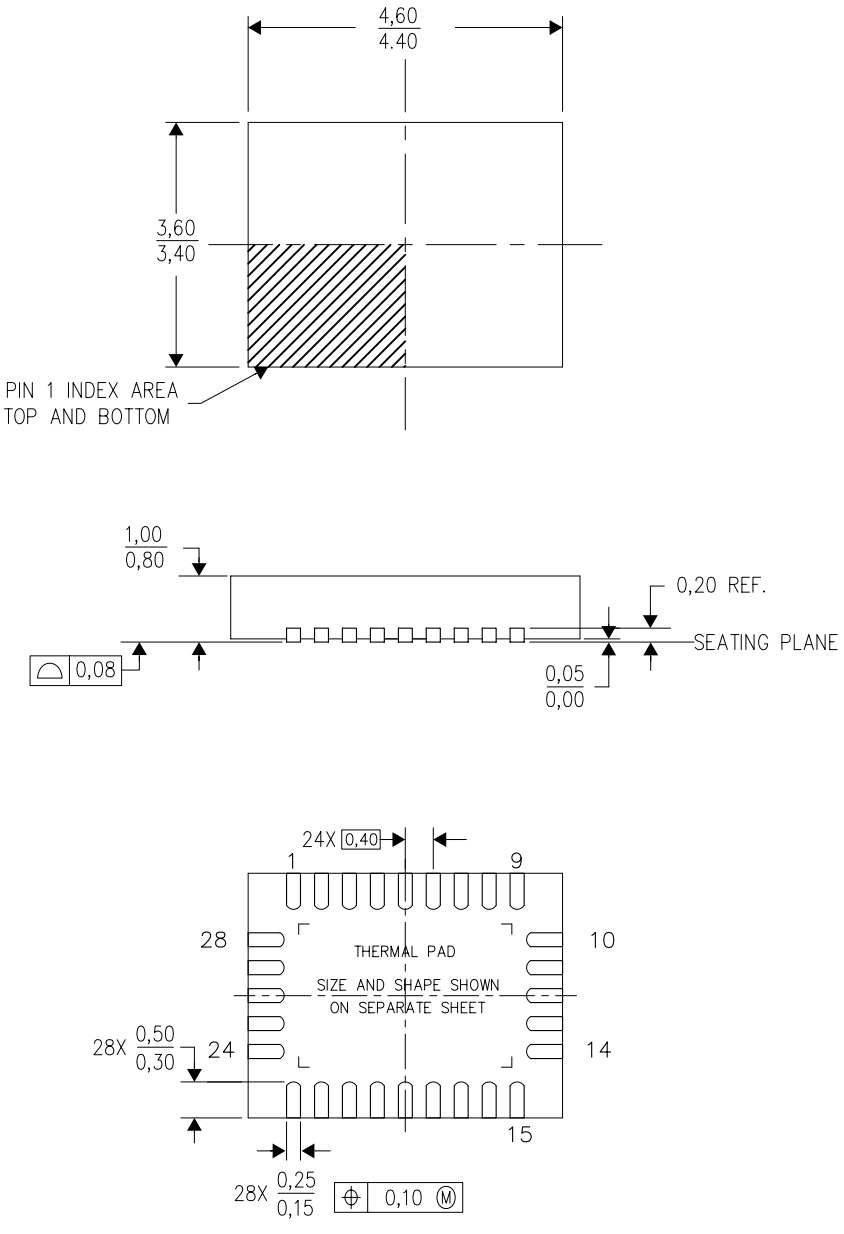
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS53915RVER	VQFN	RVE	28	3000	367.0	367.0	35.0
TPS53915RVET	VQFN	RVE	28	250	210.0	185.0	35.0

RVE (R–PVQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD



4211382/B 05/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–220.

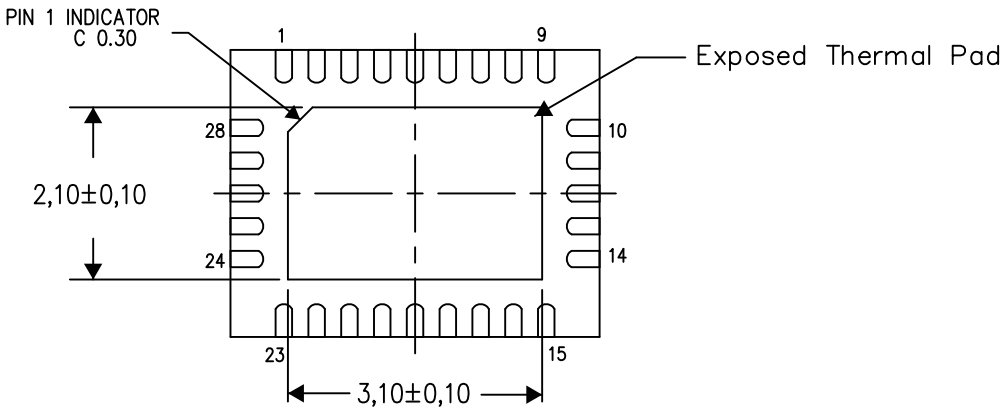
RVE (R–PVQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

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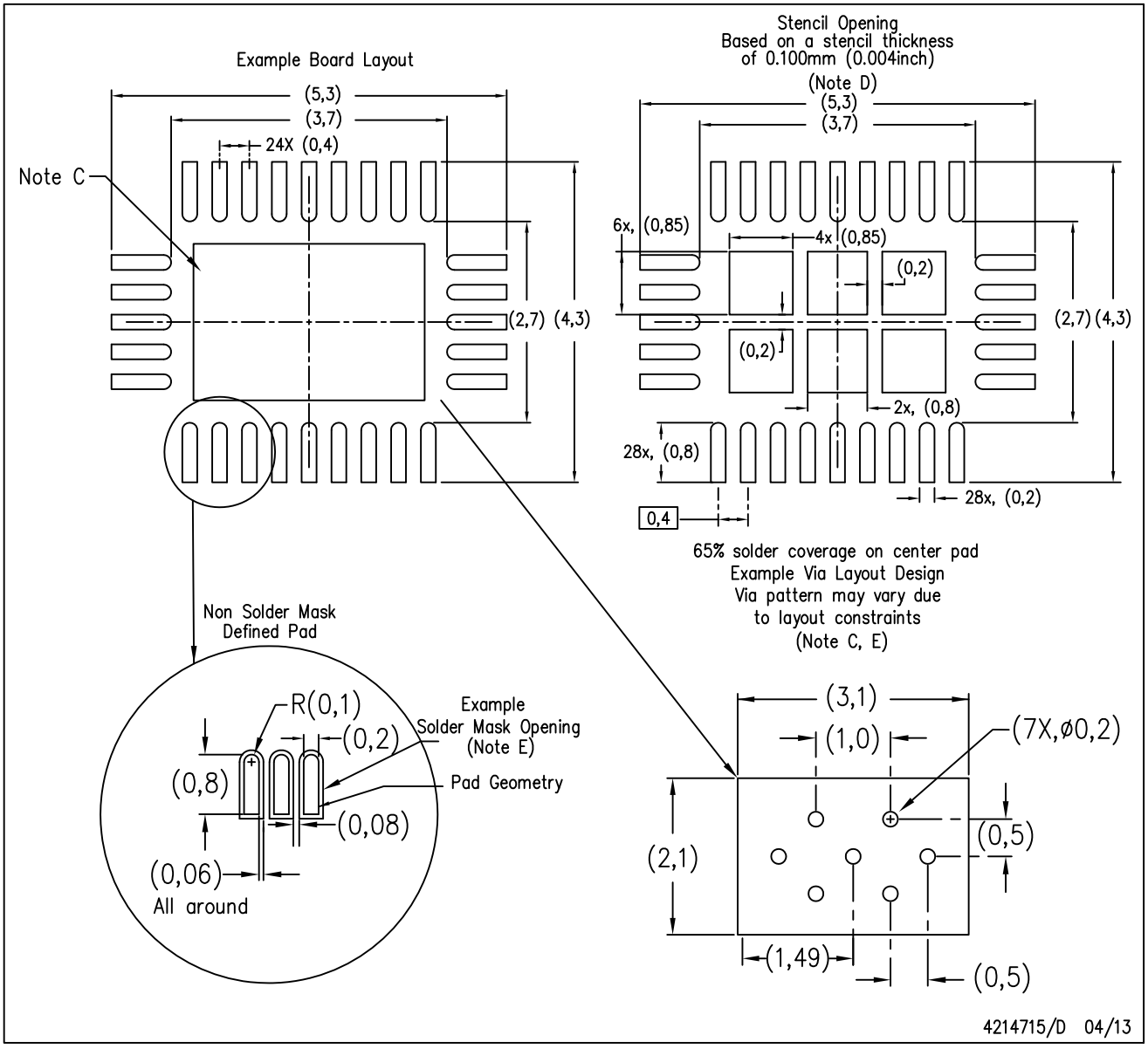
NOTE: All linear dimensions are in millimeters

RVE (R–PWQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Electroformed stencils offer adequate release at thicker values/lower Area Ratios. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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